



# Z87H3-LM

## Shark Bay

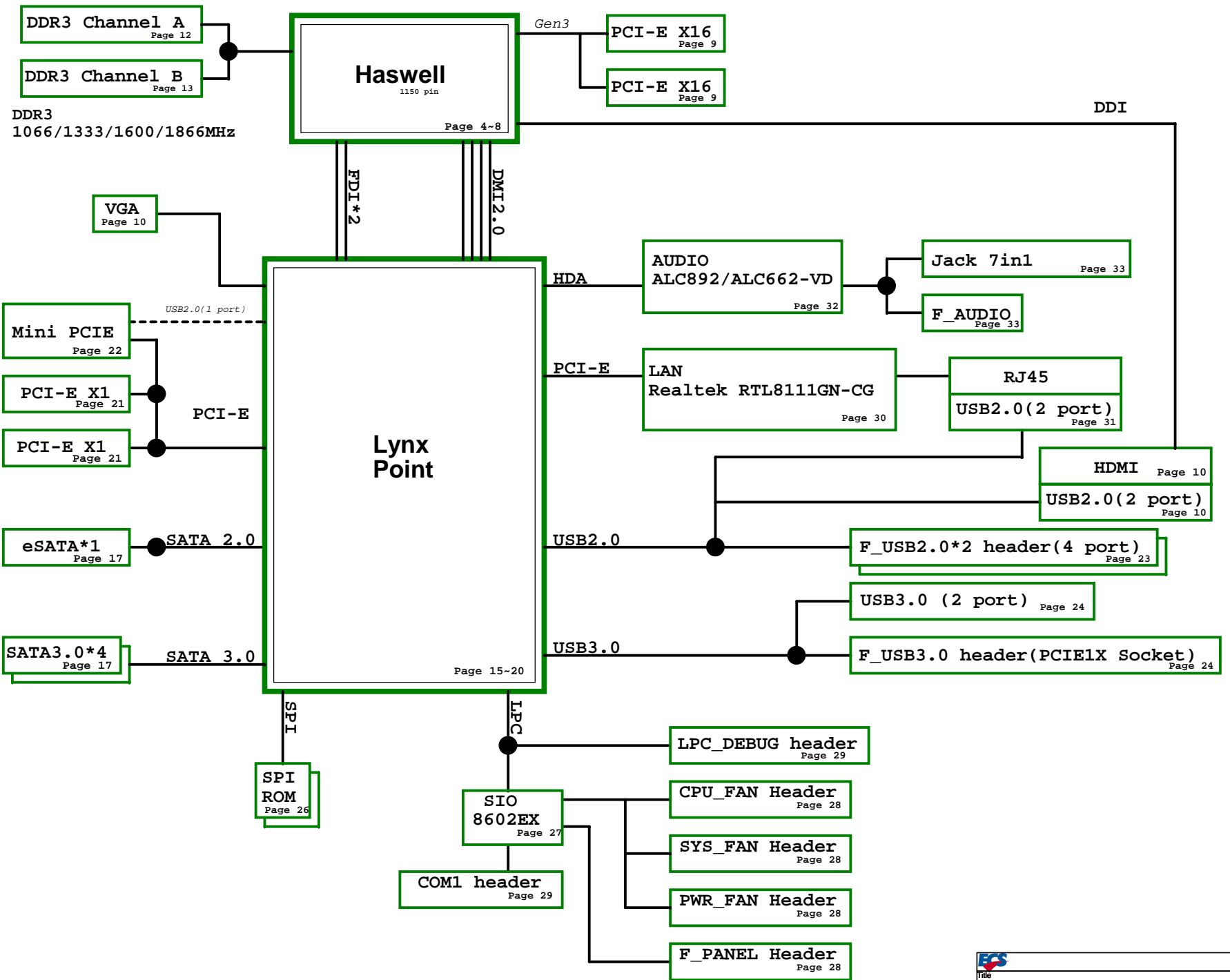
Rev:1.0..

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Job	Signature	Date
Schematics Designer	Smrk Lin	20121126
Layout		
Approval		

PCB STACK: L1:TOP  
L2:PWR  
L3:GND  
L4:BOTTOM



PCH-GPIO function

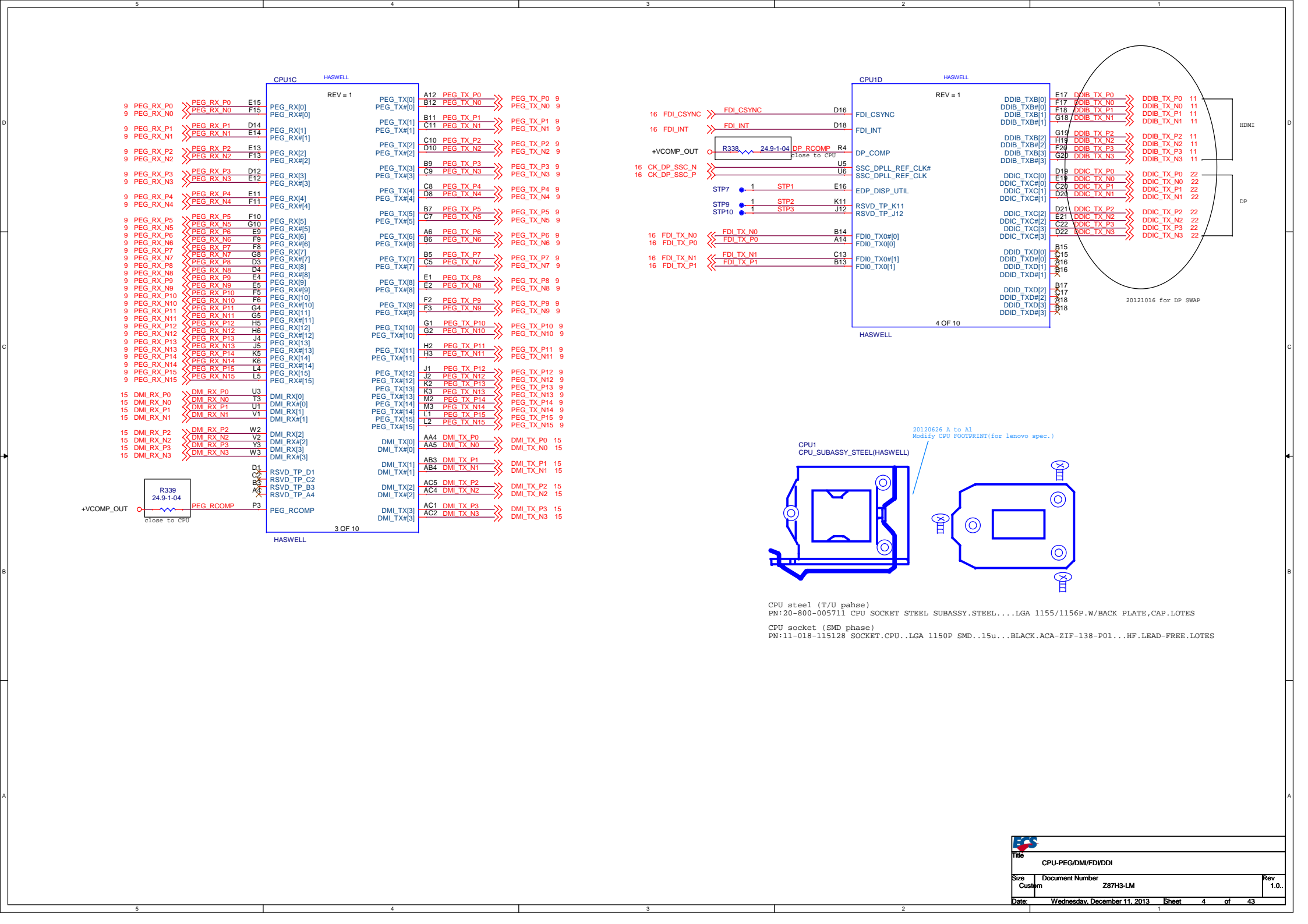
Pin Name	Power Well	Usage	Default Status	Boot Set
GPIO2	VCC3	(OC LED-WHITE)	GPI	GPO
GPIO4	VCC3	(OC LED-BLUE)	GPI	GPO
GPIO5	VCC3	(OC LED-PURPLE)	GPI	GPO
GPIO16	VCC3	(OC LED-RED)	GPI	GPO
GPIO13	3VSB	PCH_GPIO13 (USB Charger CTL1)	GPI	GPO
GPIO14	3VSB	PCH_LED1	OC7#	GPO
GPIO15	3VSB	PCIE16X_RST_L	GPO	GPI
GPIO22	VCC3	SW_CLR_CMOS	GPI	GPI
GPIO24	3VSB	ME disable	GPO	GPO
GPIO25	3VSB	PCH_GPIO25 (USB Charger CTL3)	PCIECLKRQ3#	GPO
GPIO26	3VSB	PCH_GPIO26 (USB Charger CTL4)	PCIECLKRQ4#	GPO
GPIO27	+ATX_3VSB	MS_GP0(Mode_Switch)	GPO	GPI
GPIO28	+ATX_3VSB	MS_GP1(Mode_Switch)	GPO	GPI
GPIO29	3VSB	PCH_GPIO29(BOM detect)	GPI	GPI
GPIO31	3VSB	PCH_GPIO31(+VDIMM select)	GPI	GPO
GPIO39	VCC3	CAS0(SEN_HEADER)	GPI	GPI
GPIO45	3VSB	LAN_DIS_L(MINI_PCIE)	PCIECLKRQ6#	GPO
GPIO48	VCC3	CAS1(SEN_HEADER)	GPI	GPI
GPIO49	VCC3	PCH_GPIO49 USB/PCIE(mSATA) DET	GPI	GPO
GPIO50	VCC3	PS2_DET	GPI	GPI
GPIO52	VCC3	PCH_GPIO52 (FP_AUD_DETECT)	GPI	GPO
GPIO54	VCC3	COM_DET	GPI	GPI
GPIO57	3VSB	MODE_CTRL(Mode_Switch)	GPI	GPI
GPIO60	3VSB	PCH_GPIO60(BOM detect)	SML0ALERT#.	GPI
GPIO64	VCC3	PCH_GPIO64(BOM detect)	CLKOUTFLEX0	GPI
GPIO65	VCC3	PCH_GPIO65(BOM detect)	CLKOUTFLEX1	GPI
GPIO66	VCC3	PCH_GPIO66(BOM detect)	CLKOUTFLEX2	GPI
GPIO73	3VSB	PCH_GPIO73	PCIECLKRQ0#	GPI
GPIO74	3VSB	PCH_GPIO74(BOM detect)	SML1ALERT#	GPI

SIO-GPIO function

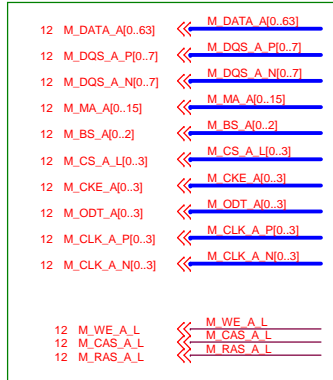
Pin Name	Power Well	Usage	Default SET
GP22	3VSB	SIO_LED0	GPIO
GP12	VCC3	PCIRST1_L	GPO

Interrupt mapping

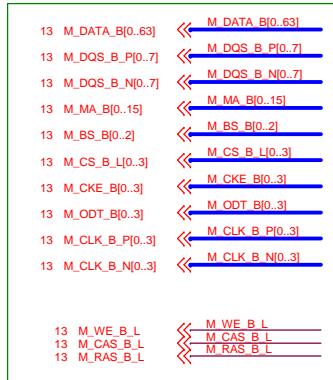
Function	INT# port	PCle*1 port	Device
LAN	INTC#	port 3	RTL8111GN
PCIE1X_1	INTB#	port 2	LPT integrate
PCIE1X_2	INTD#	port 4	LPT integrate
mini-PCIE	INTB#	port 6	LPT integrate
SATA	INTB#	N/A	LPT integrate







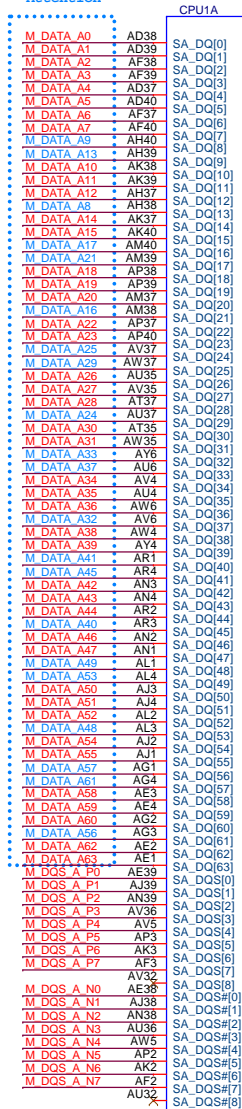
DDR3 CH.A



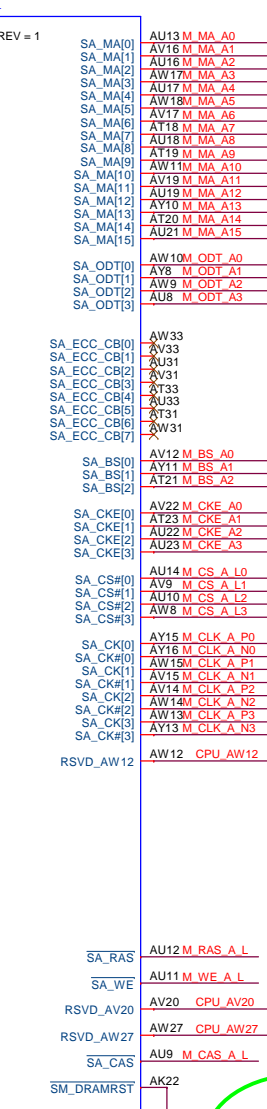
DDR3 CH.B

6,12,13 DDR3\_DRAMRST\_L << DDR3\_DRAMRST\_L

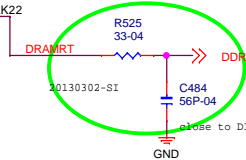
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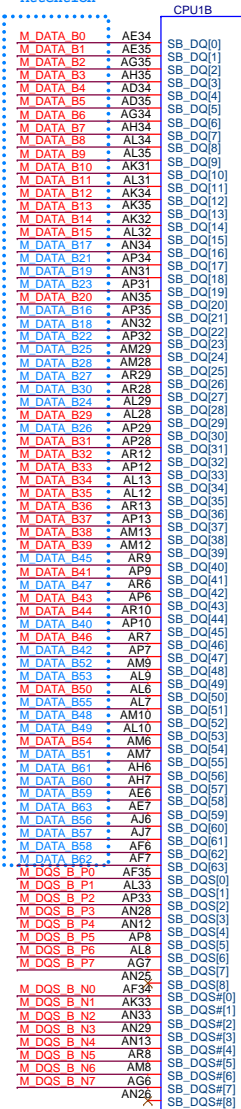
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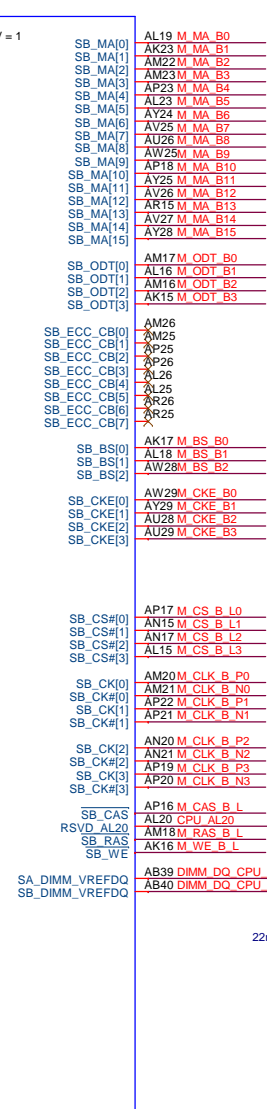
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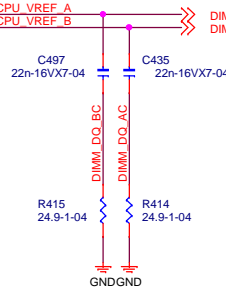
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HASWELL

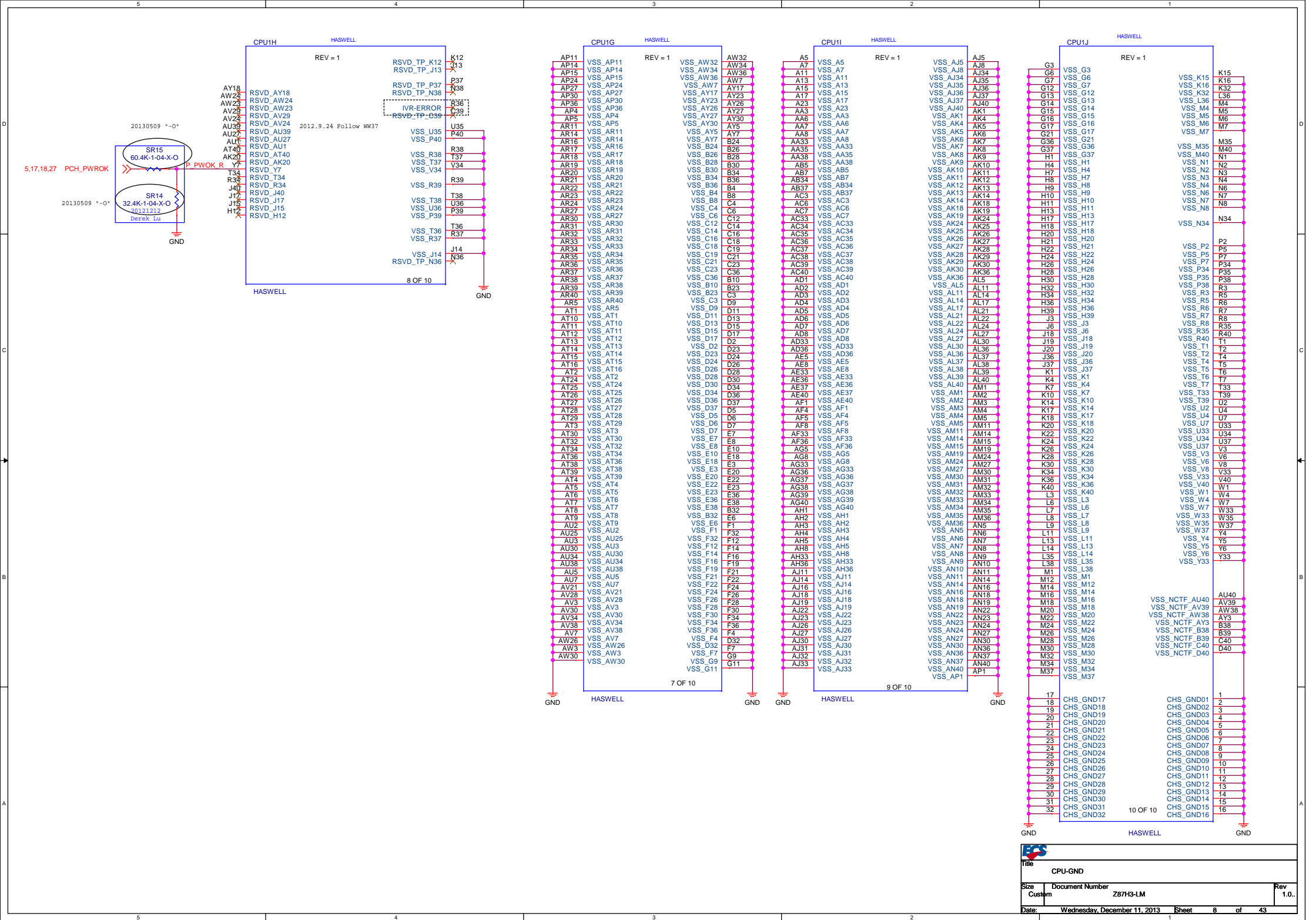


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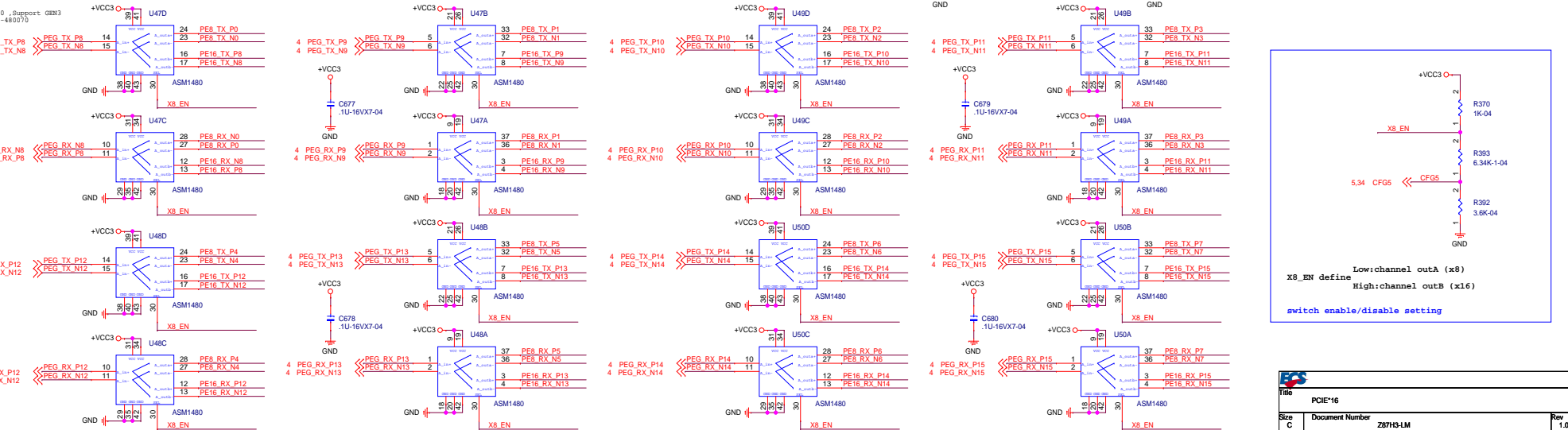
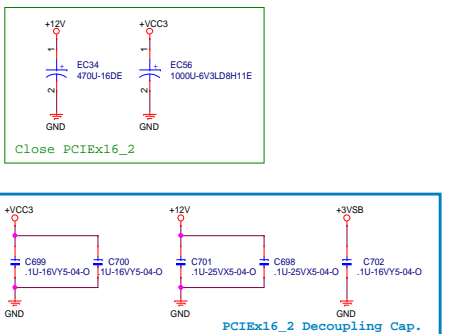
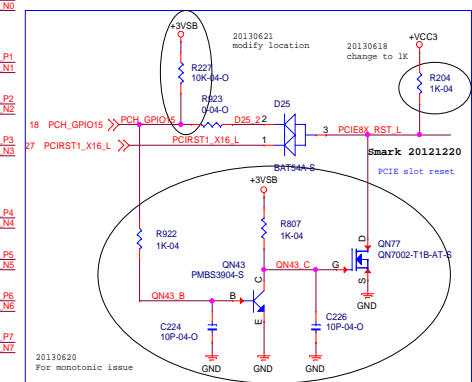
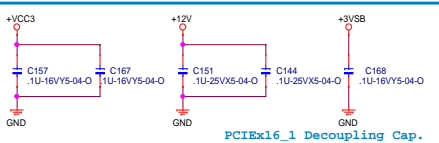
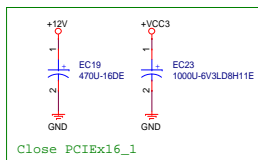
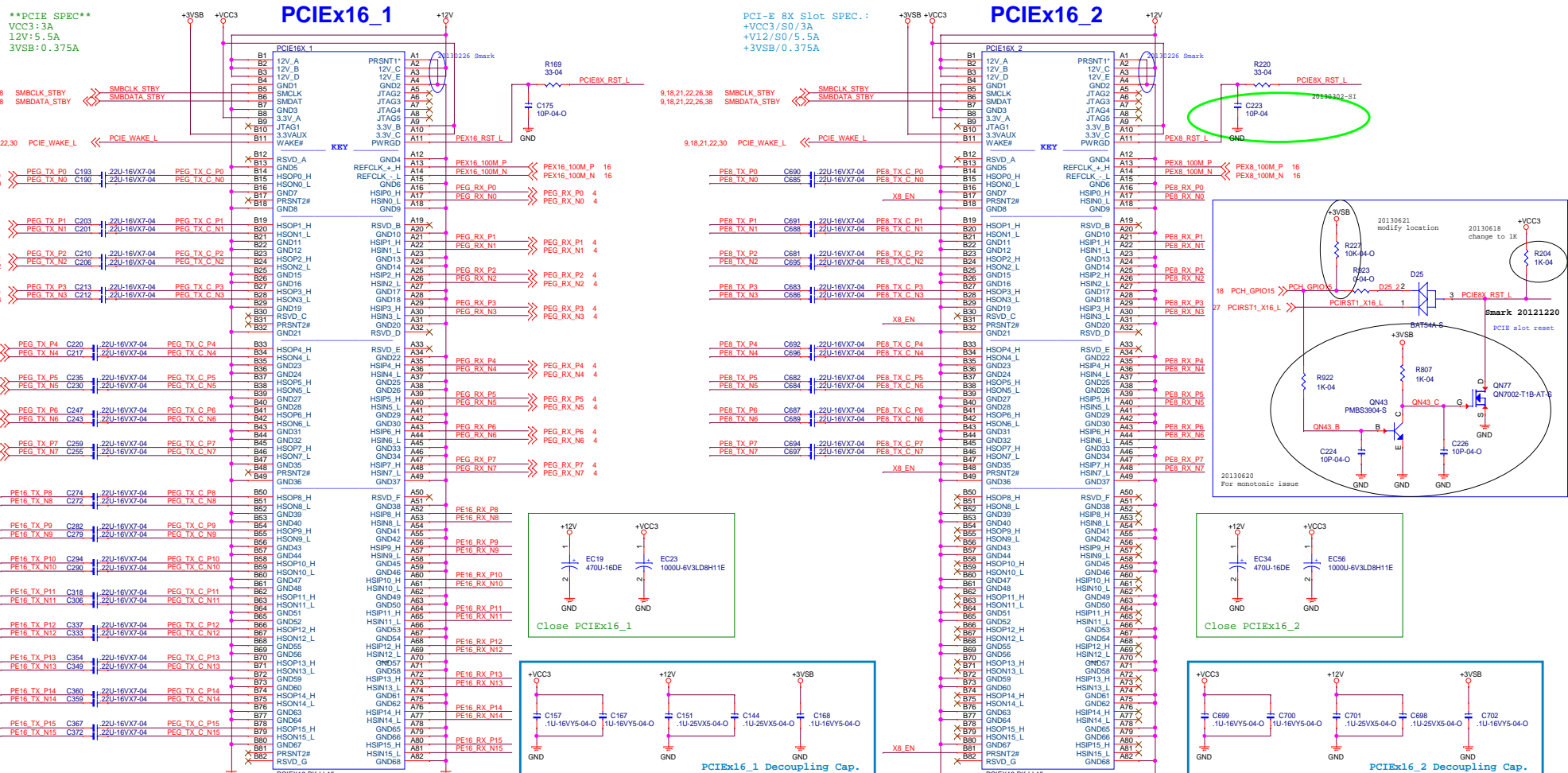


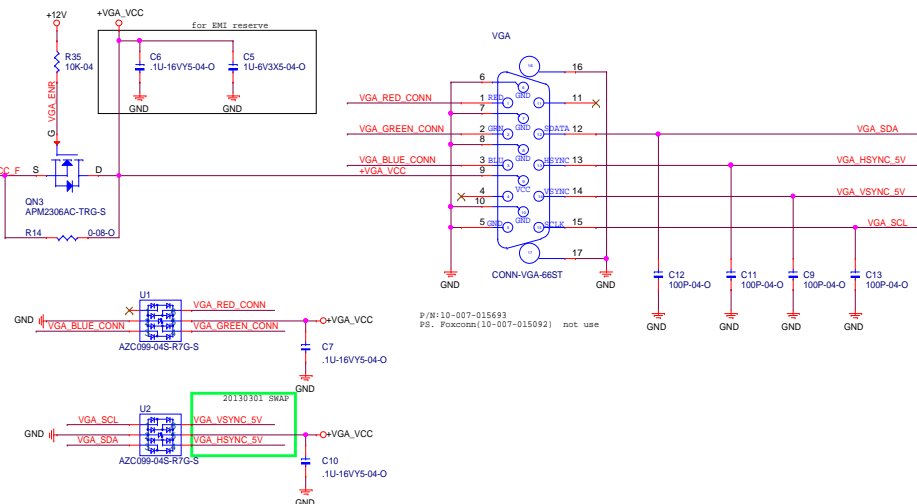
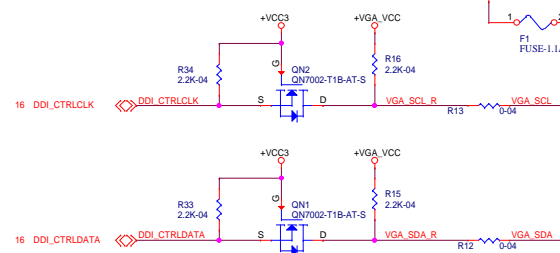
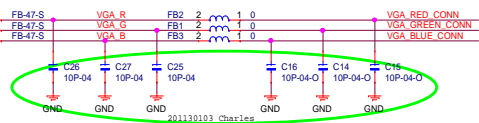
\*\*PCIe SPEC\*\*  
VCC3: 3A  
12V: 5.5A  
3VSB: 0.375A

## PCIEx16\_1

PCI-E 8X Slot SPEC.:  
+VCC3/S0/3A  
+V12/S0/5.5A  
+3VSB/0.375A

## PCIEx16\_2





Pin 1 to 27 connection diagram for USB-HDMI Type A connector. The diagram shows the connection of various signals between the connector pins and the board components.

Connector Pin	Signal	Board Component
1	HDMI TX2 DP C	2
2	HDMI TX2 DN C	3
3	HDMI TX1 DP C	4
4	HDMI TX1 DN C	5
5	HDMI TX0 DP C	6
6	HDMI TX0 DN C	7
7	HDMI TX2 DP C	8
8	HDMI TX2 DN C	9
9	HDMI TX1 DP C	10
10	HDMI TX1 DN C	11
11	HDMI TX0 DP C	12
12	HDMI TX0 DN C	13
13	HDMI CLK DP C	14
14	HDMI CLK DN C	15
15	HDMI SCL	16
16	HDMI SDA	17
17	HDMI HPD_ASL	18
18	HDMI HPD_ASL	19
19	HDMI HPD_ASL	20
20	HDMI HPD_ASL	21
21	HDMI HPD_ASL	22
22	HDMI HPD_ASL	23
23	HDMI HPD_ASL	24
24	HDMI HPD_ASL	25
25	HDMI HPD_ASL	26
26	HDMI HPD_ASL	27
27	HDMI HPD_ASL	28

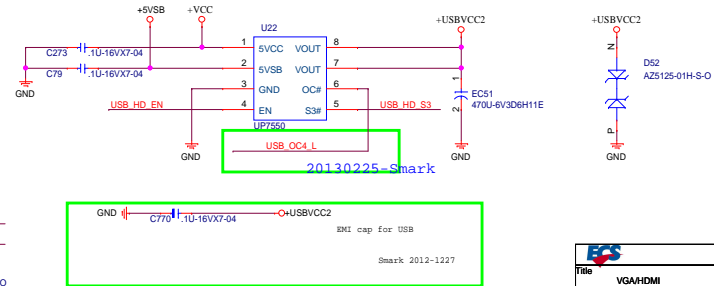
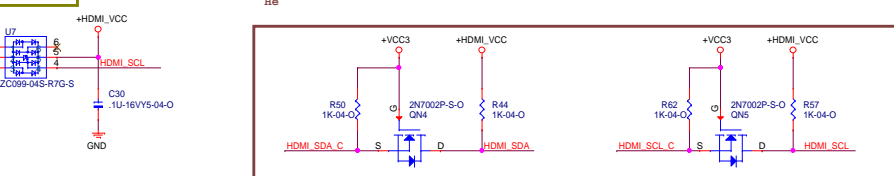
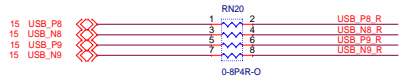
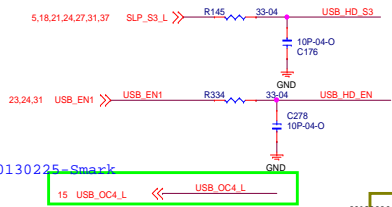
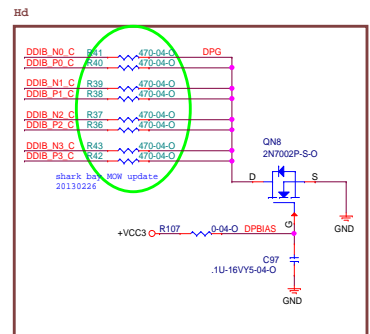
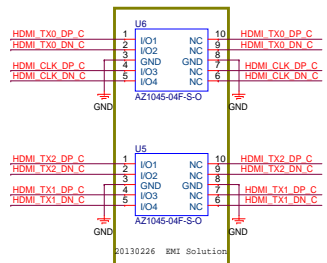
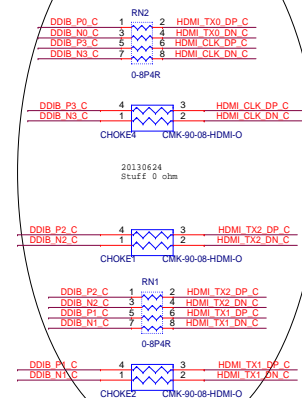
Additional connections shown in the diagram:

- Pin 20: +USBVCC2
- Pin 21: USB N8\_R
- Pin 22: USB P8\_R
- Pin 23: USB N9\_R
- Pin 24: USB P9\_R
- Pin 25: USB N9\_R
- Pin 26: USB P9\_R
- Pin 27: GND

Legend:

- 1: GND
- 2: GND
- 3: GND
- 4: GND
- 5: GND
- 6: GND
- 7: GND
- 8: GND
- 9: GND
- 10: GND
- 11: GND
- 12: GND
- 13: GND
- 14: GND
- 15: GND
- 16: GND
- 17: GND
- 18: GND
- 19: GND
- 20: GND
- 21: GND
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- 23: GND
- 24: GND
- 25: GND
- 26: GND
- 27: GND
- 28: GND

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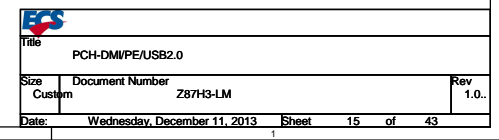
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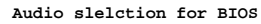




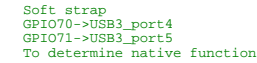


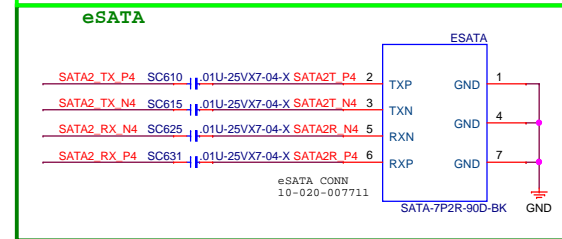
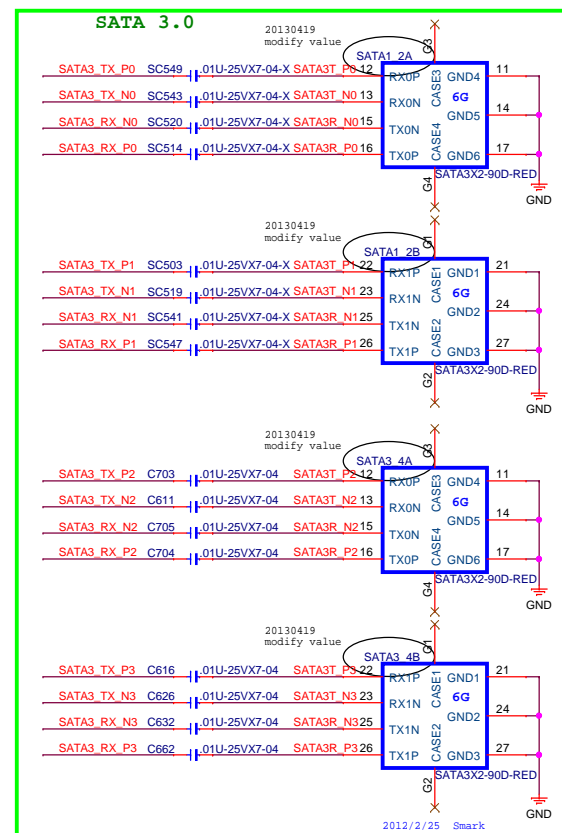
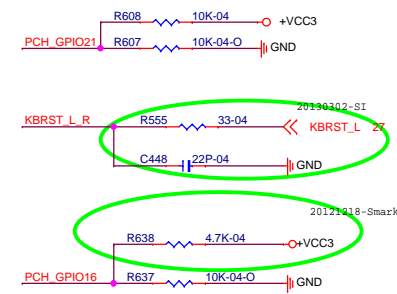
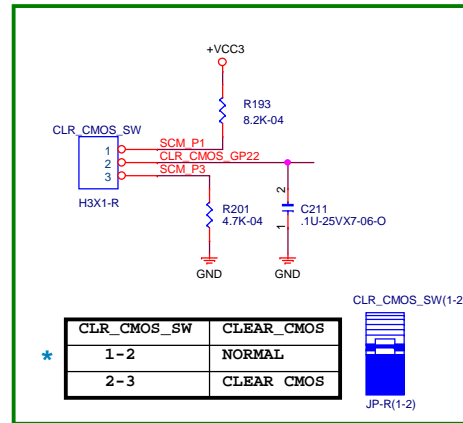
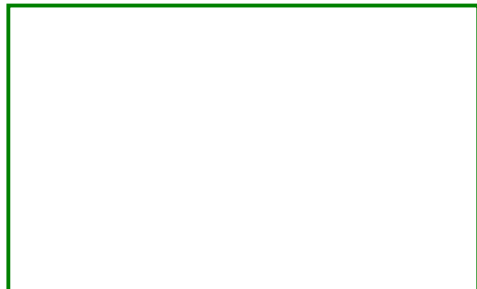
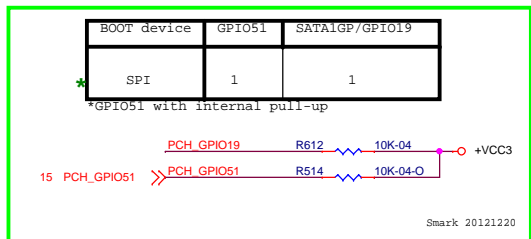
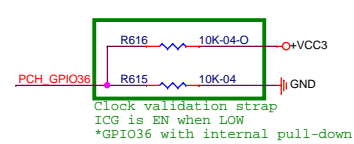
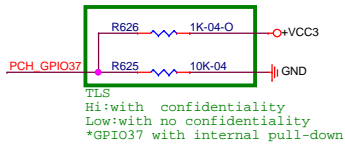
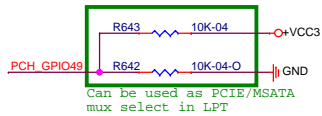
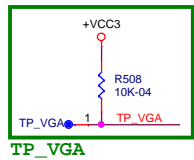
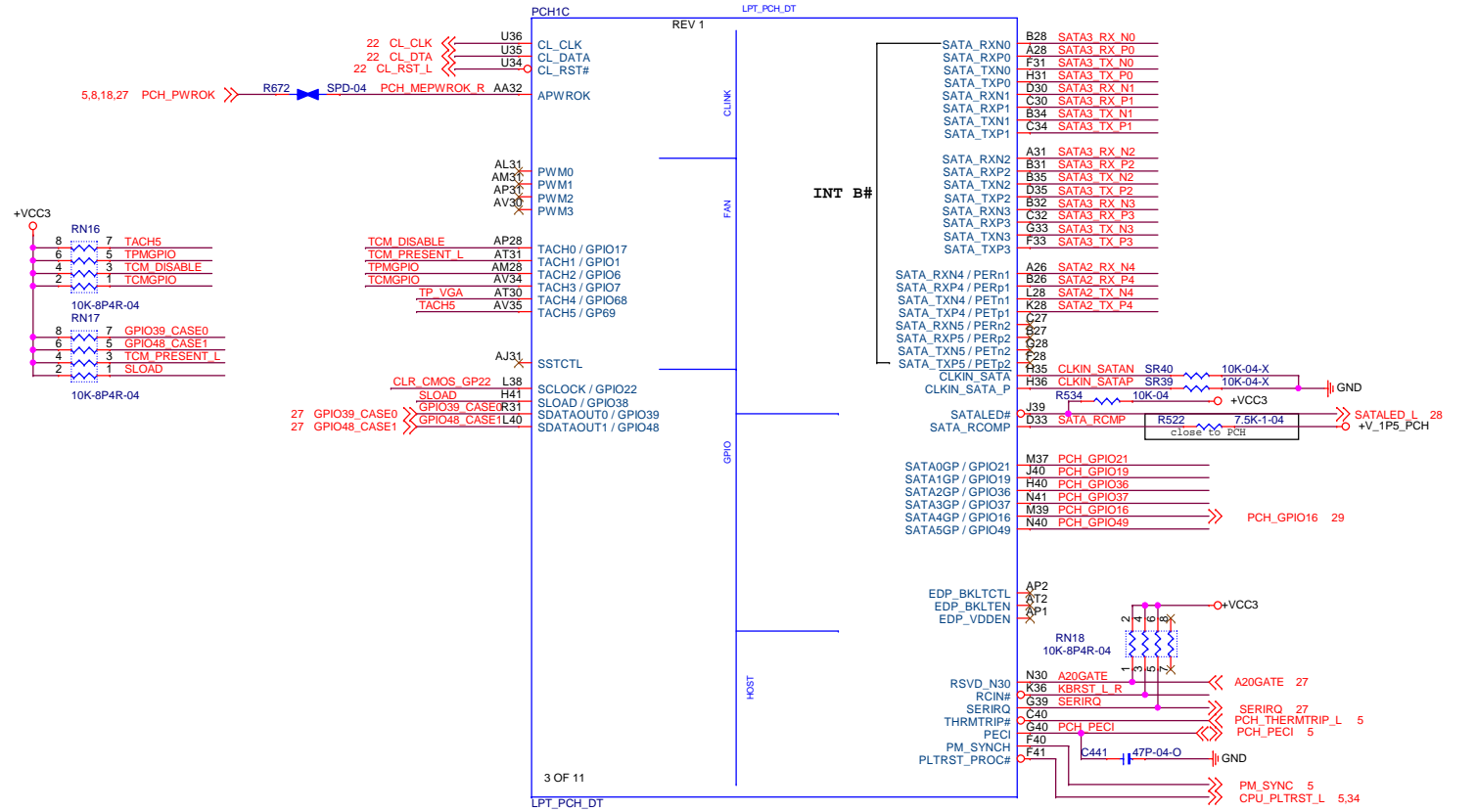


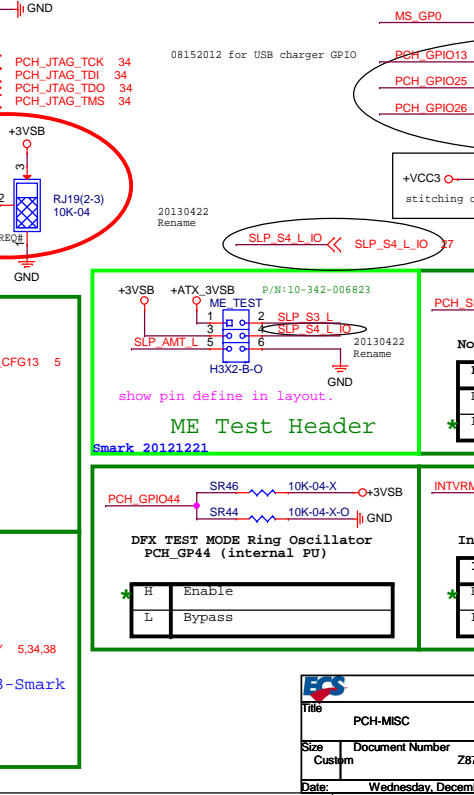
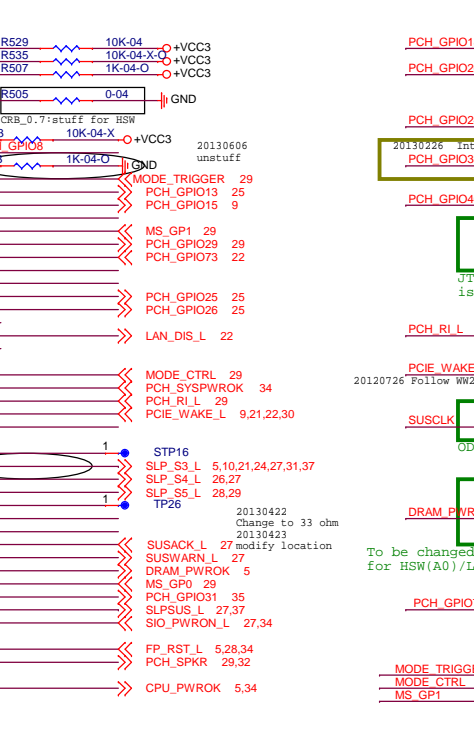
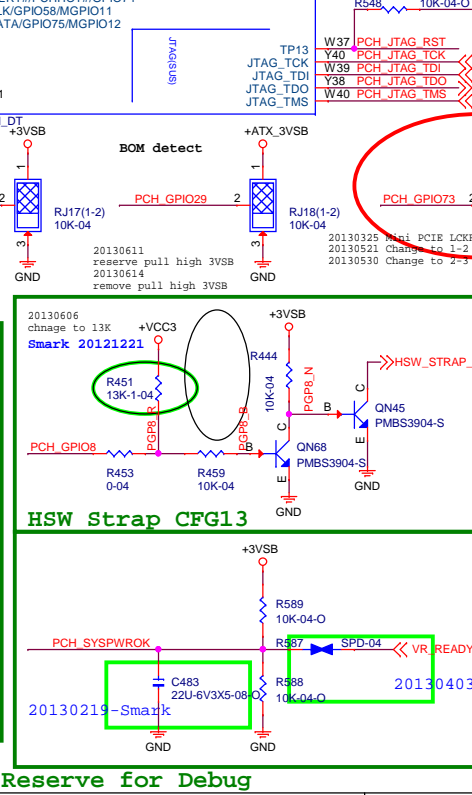
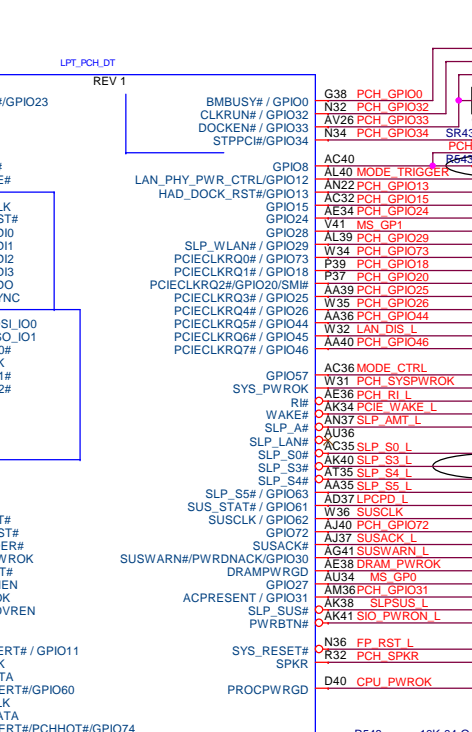
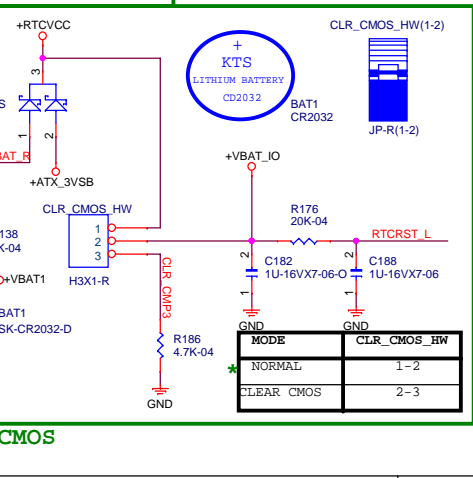
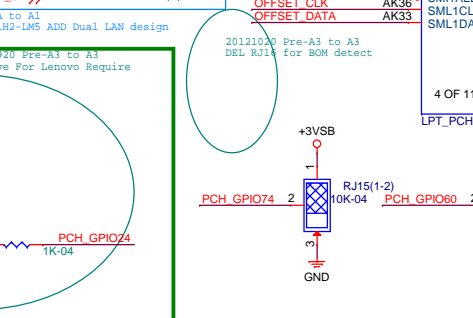
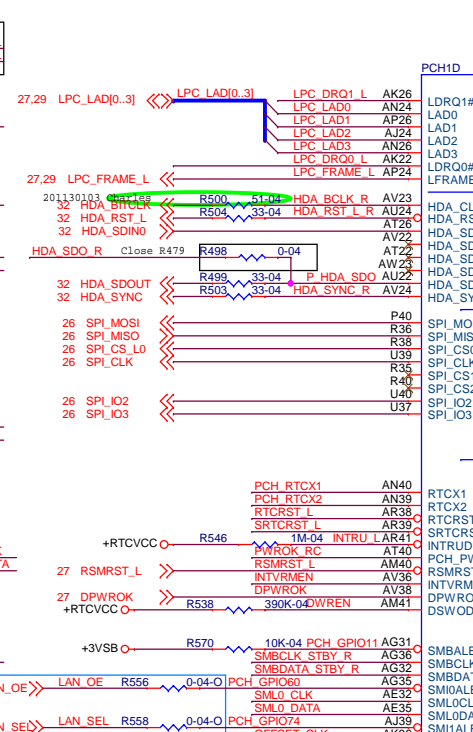
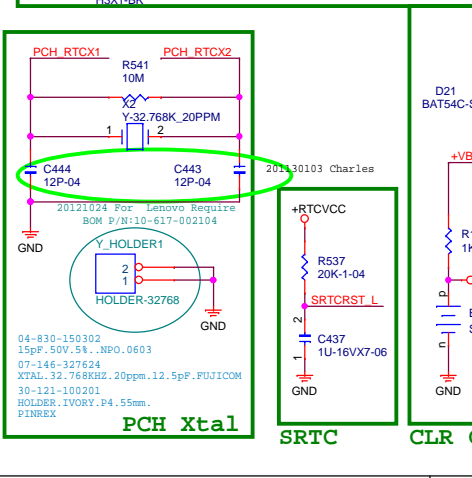
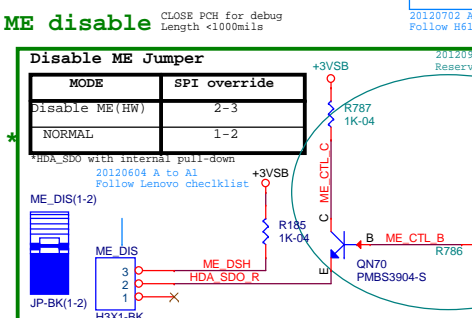
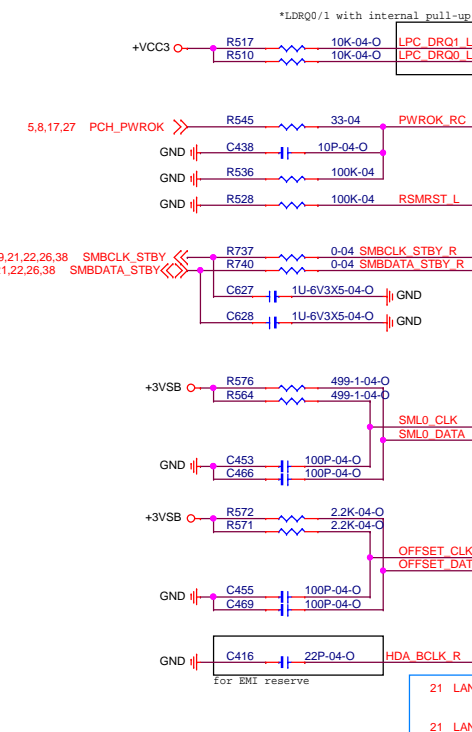




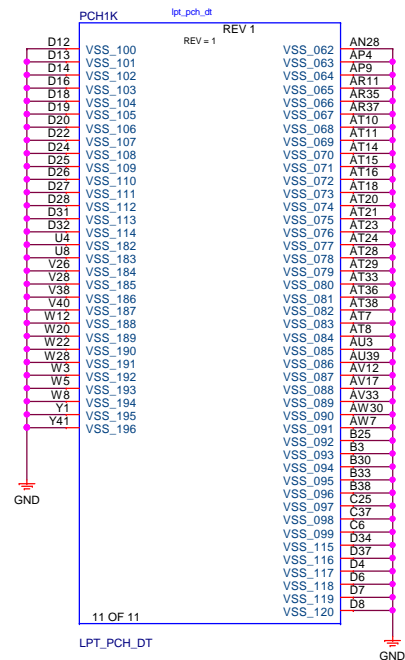
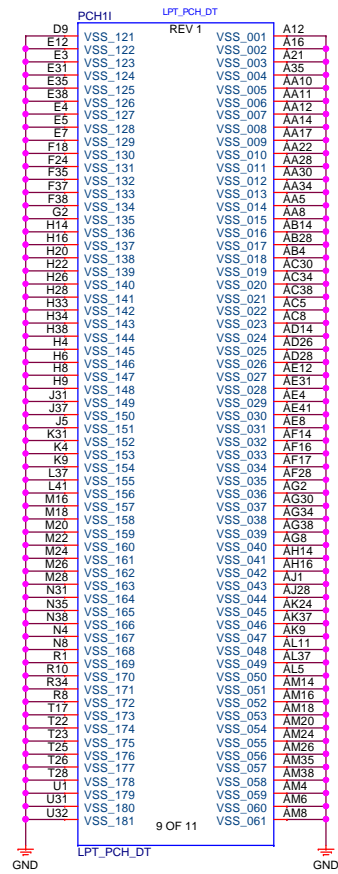
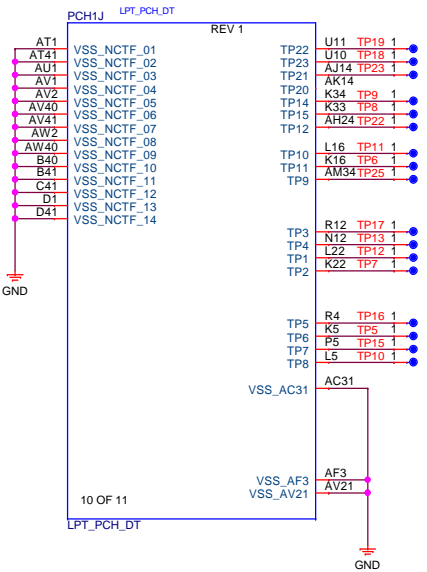
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ALC662	2-3

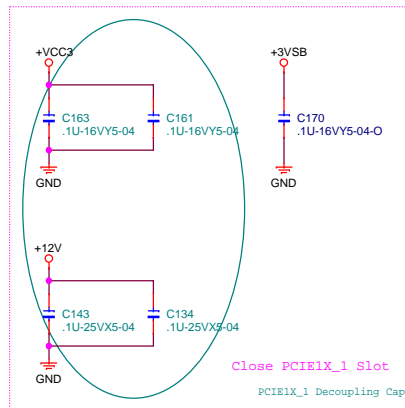
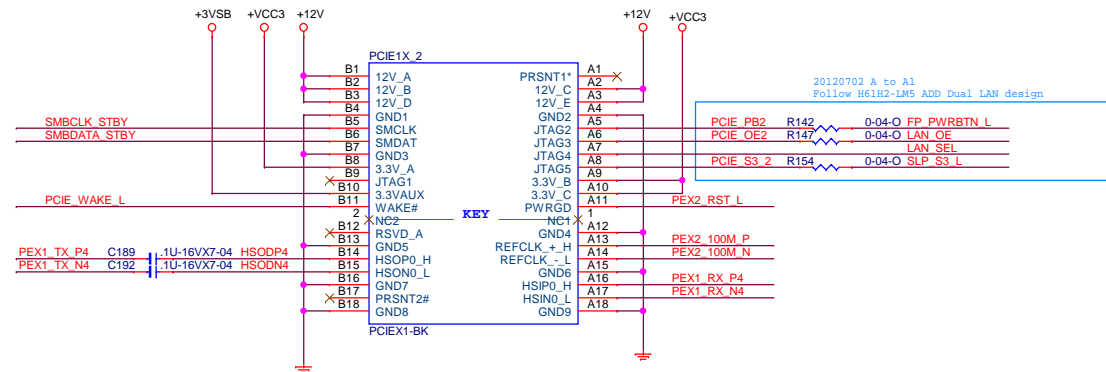
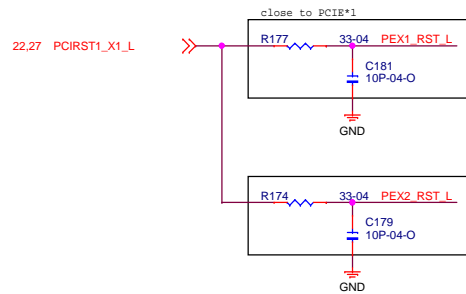
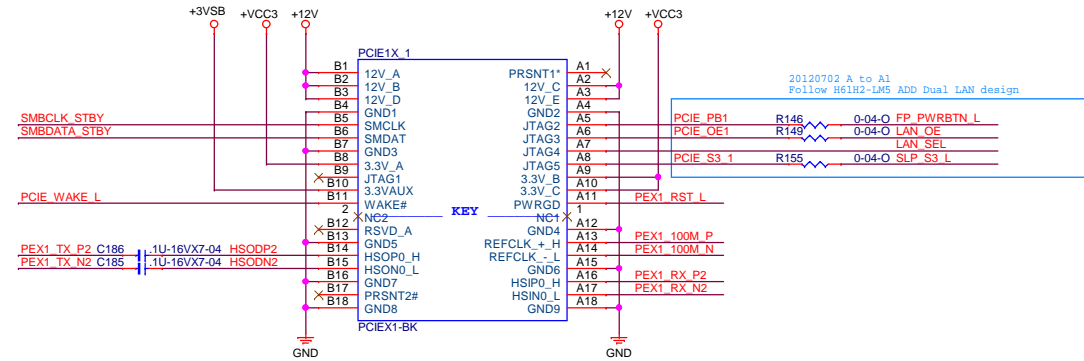
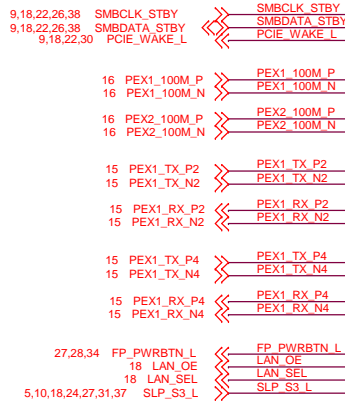




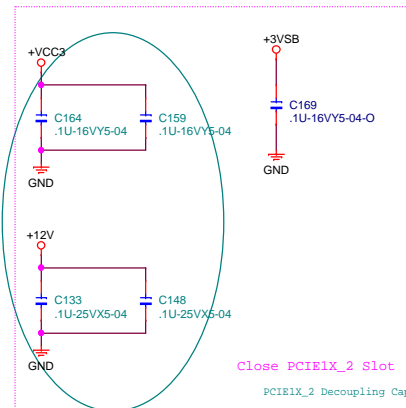




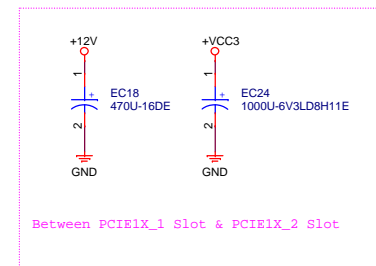
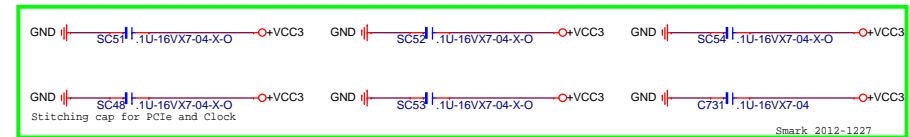




20121107 Pre-A3 to A3  
form Reserve to Add  
For Lenovo Require



20121107 Pre-A3 to A3  
form Reserve to Add  
For Lenovo Require





## MINI\_PCIE

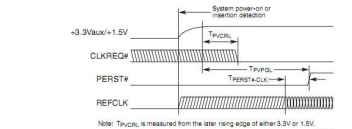
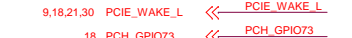
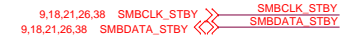
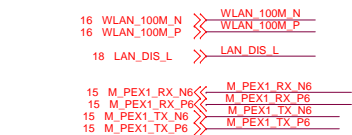
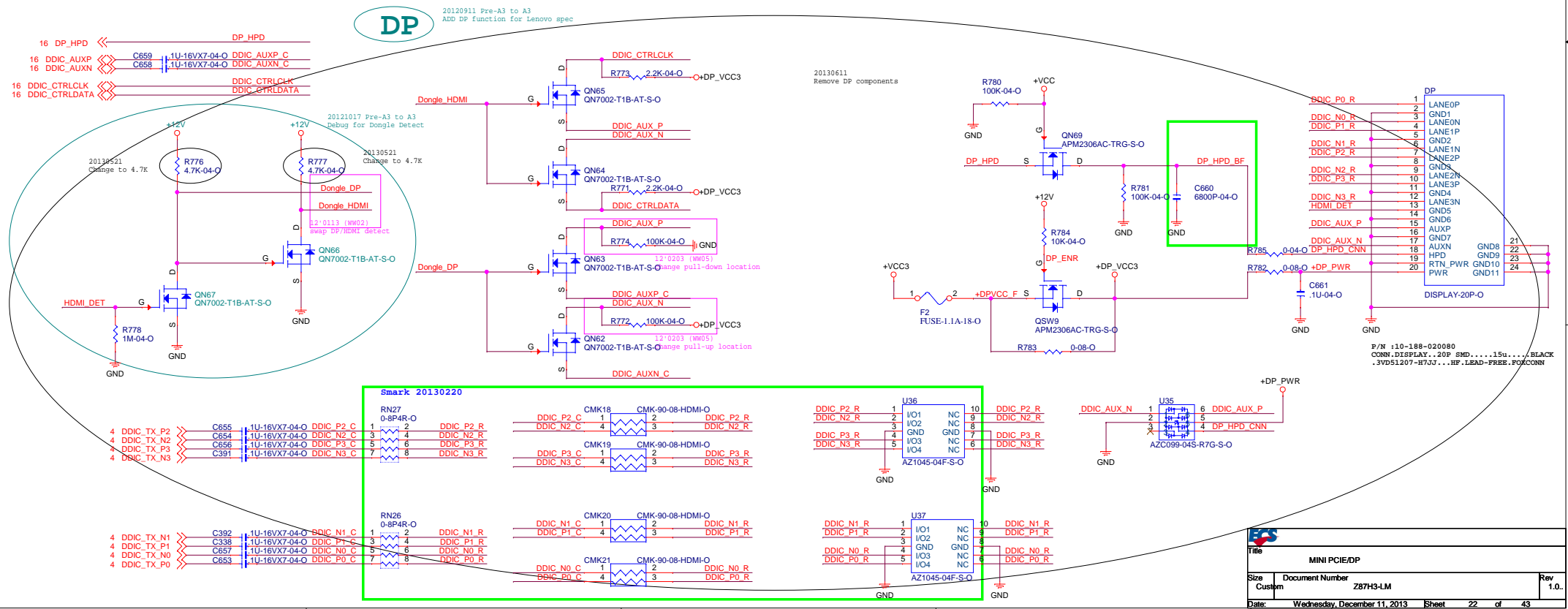
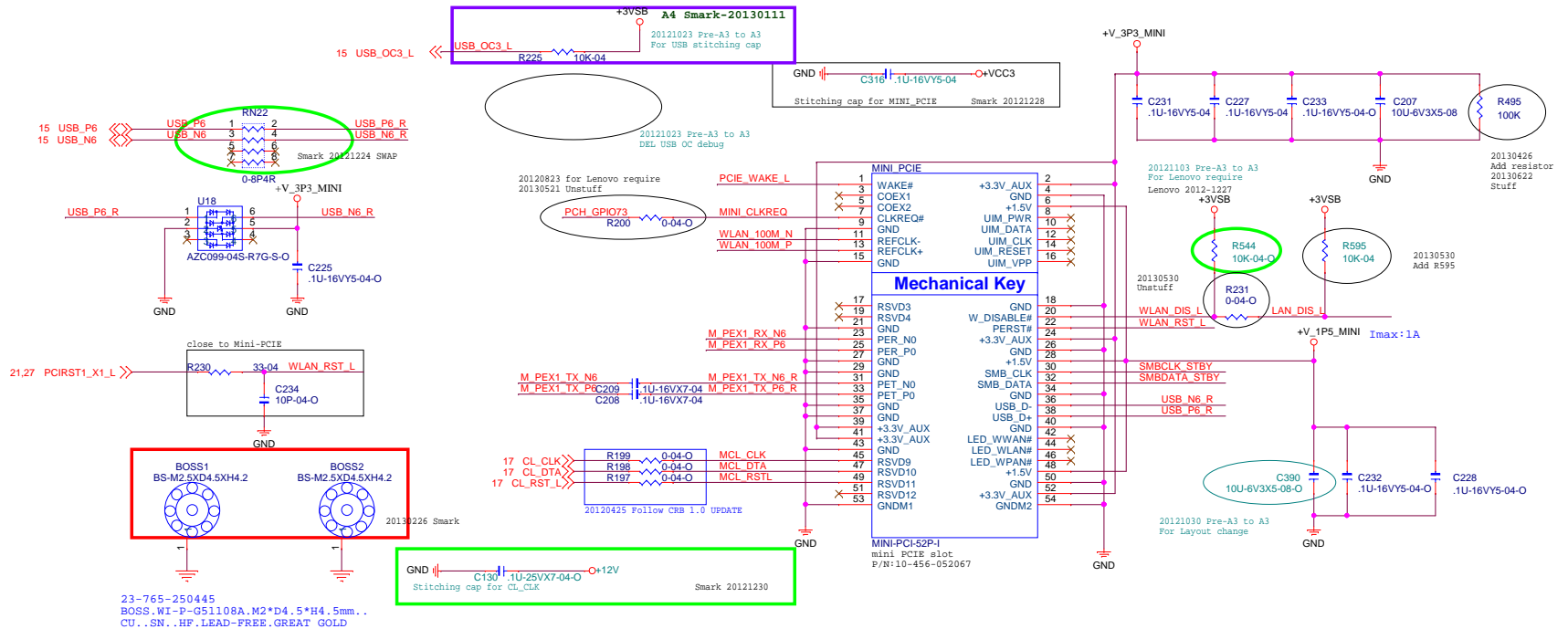


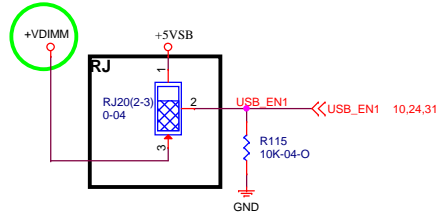
Figure 3-1: Power-Up CLKREQ# Timing

Symbol	Parameter	Min	Max	Units
$T_{PWR}$	Power Valid to CLKREQ# Output active		100	$\mu$ s
$T_{PVDL}$	Power Valid to PERST# Input inactive	1		ms
$T_{RESTRCLK}$	REFCLK stable before PERST# inactive	100		$\mu$ s



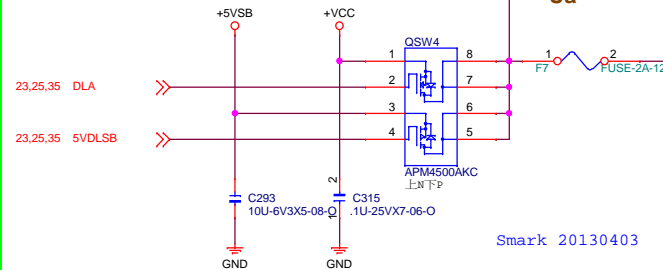


	uP7550 Enable use	RJ	S4/S5 USB_5V_DUAL	
★	+VDIMM	0ohm (2-3)	0 Volt	Lenovo S4/S5 w/o USB_5V_DUAL
	5VSB	0ohm (1-2)	5 Volt	

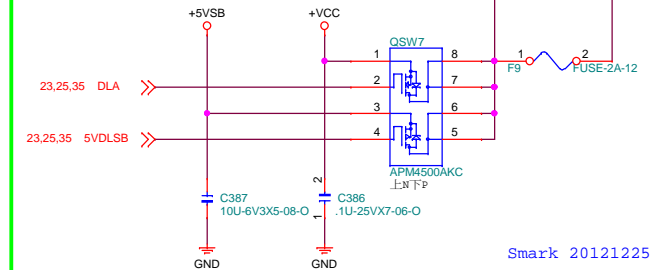


2012/12/11 Smark

### +USBVCC8

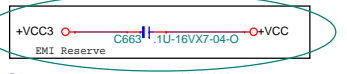
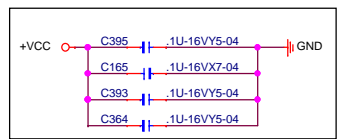
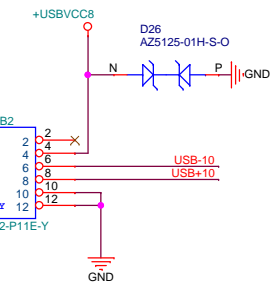
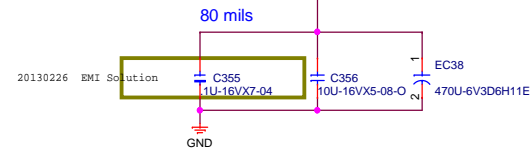
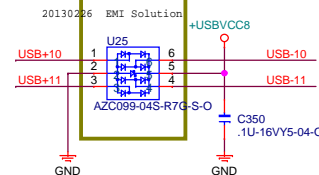
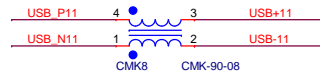
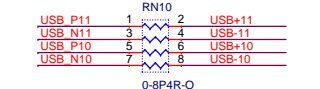
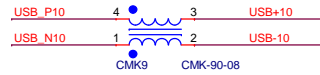


### +USBVCC6

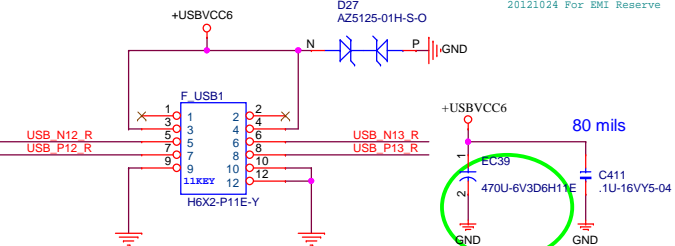
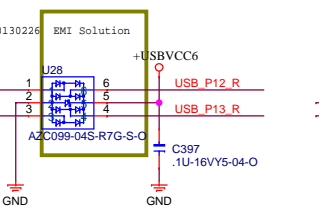


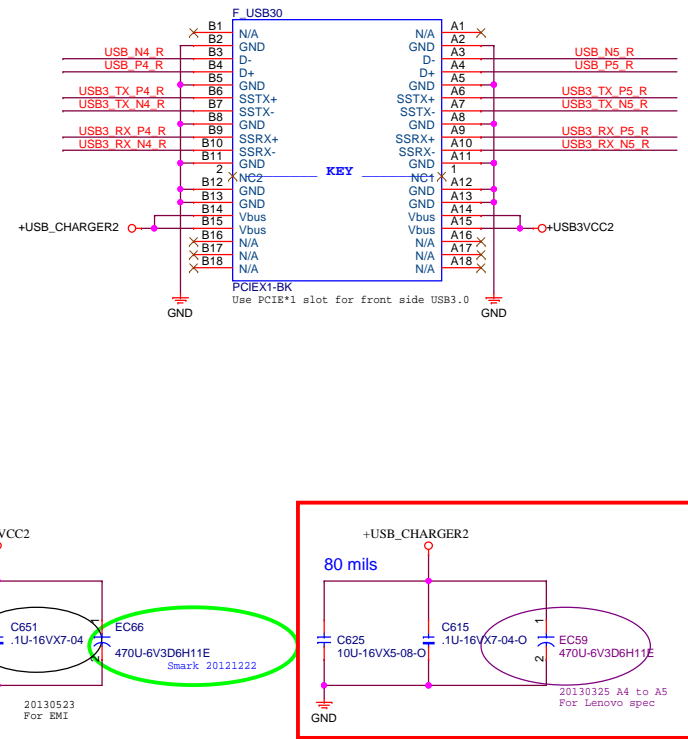
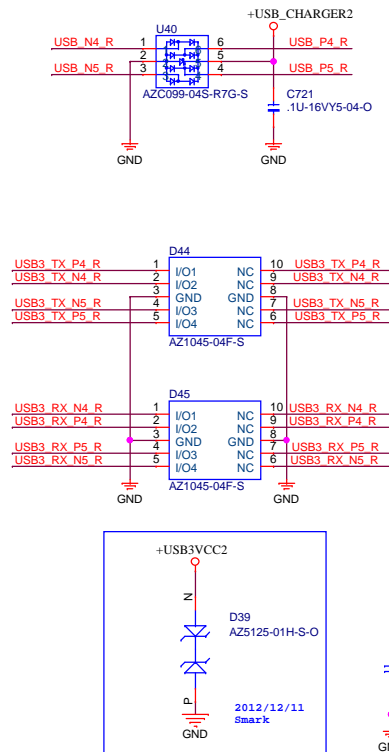
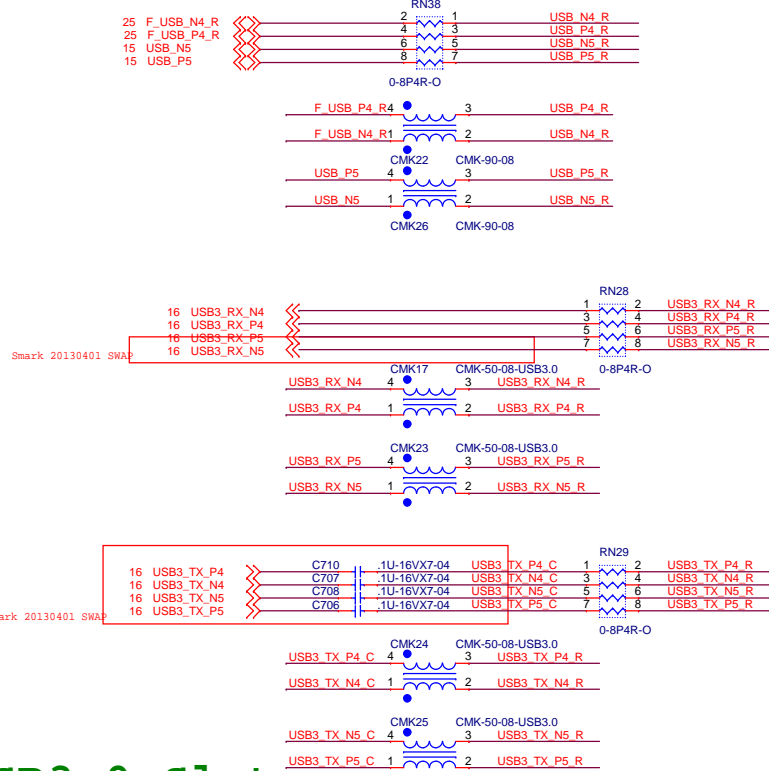
## USB2.0 header

- 15 USB\_N10
- 15 USB\_P10
- 15 USB\_N11
- 15 USB\_P11



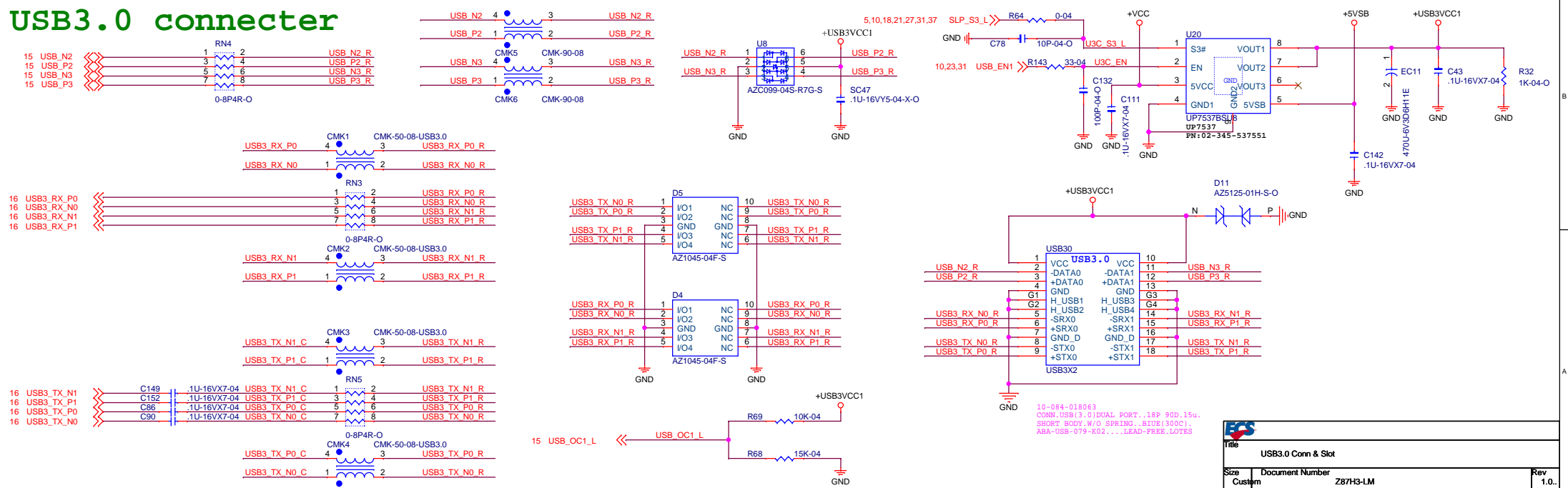
20121024 For EMI Reserve





# USB3.0 slot

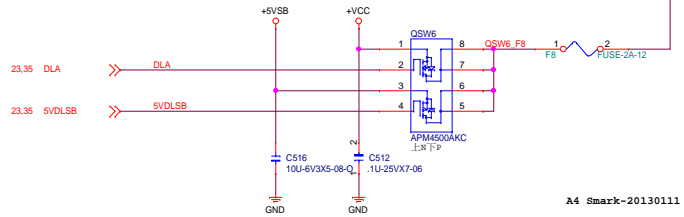
# USB3.0 connector



Title			USB3.0 Conn & Slot
Size	Document Number	Z87H3-LM	
Custom			
Date:	Wednesday, December 11, 2013	Sheet	24 of 43

# +USB3VCC2

15 USB\_N4 <> USB\_N4  
15 USB\_P4 <> USB\_P4  
24 F\_USB\_N4\_R <> F\_USB\_N4\_R  
24 F\_USB\_P4\_R <> F\_USB\_P4\_R



A4 Smark-20130111

# USB Charger GPIO

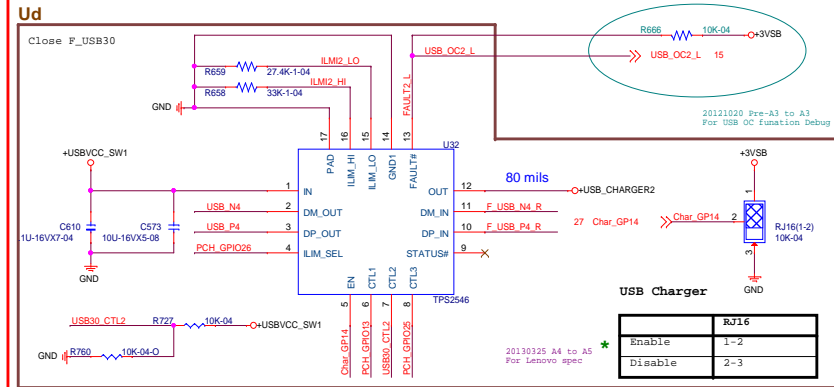
18 PCH\_GPIO13 <> PCH\_GPIO13  
18 PCH\_GPIO25 <> PCH\_GPIO25  
18 PCH\_GPIO26 <> PCH\_GPIO26

## TPS2543 Control Mode

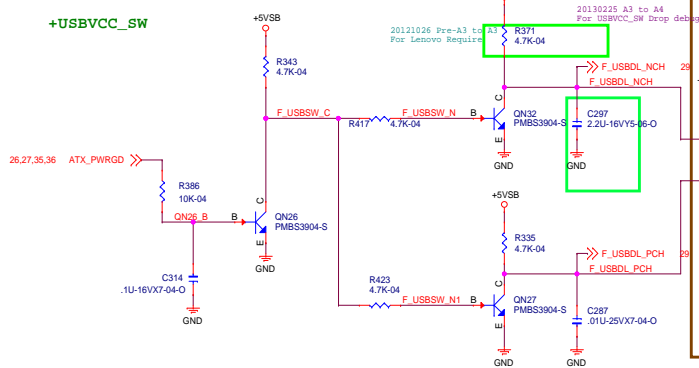
Input Logic Level				Control Mode	
BP1013	CTL2	BP1025	BP1026	System Status	Charging Mode
0	1	1	0	S4/S5	DCP
1	1	1	0	S0/S3	SDP

20130606 20121031Pre-A3 to A3  
modify to 1 Change S0 to SDP Mode for Lenovo spec

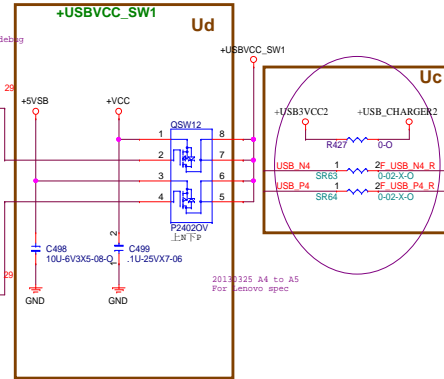
## USB3.0 Slot of USB2.0 Charger Circuit



# +USBVCC\_SW



# +USBVCC\_SW1

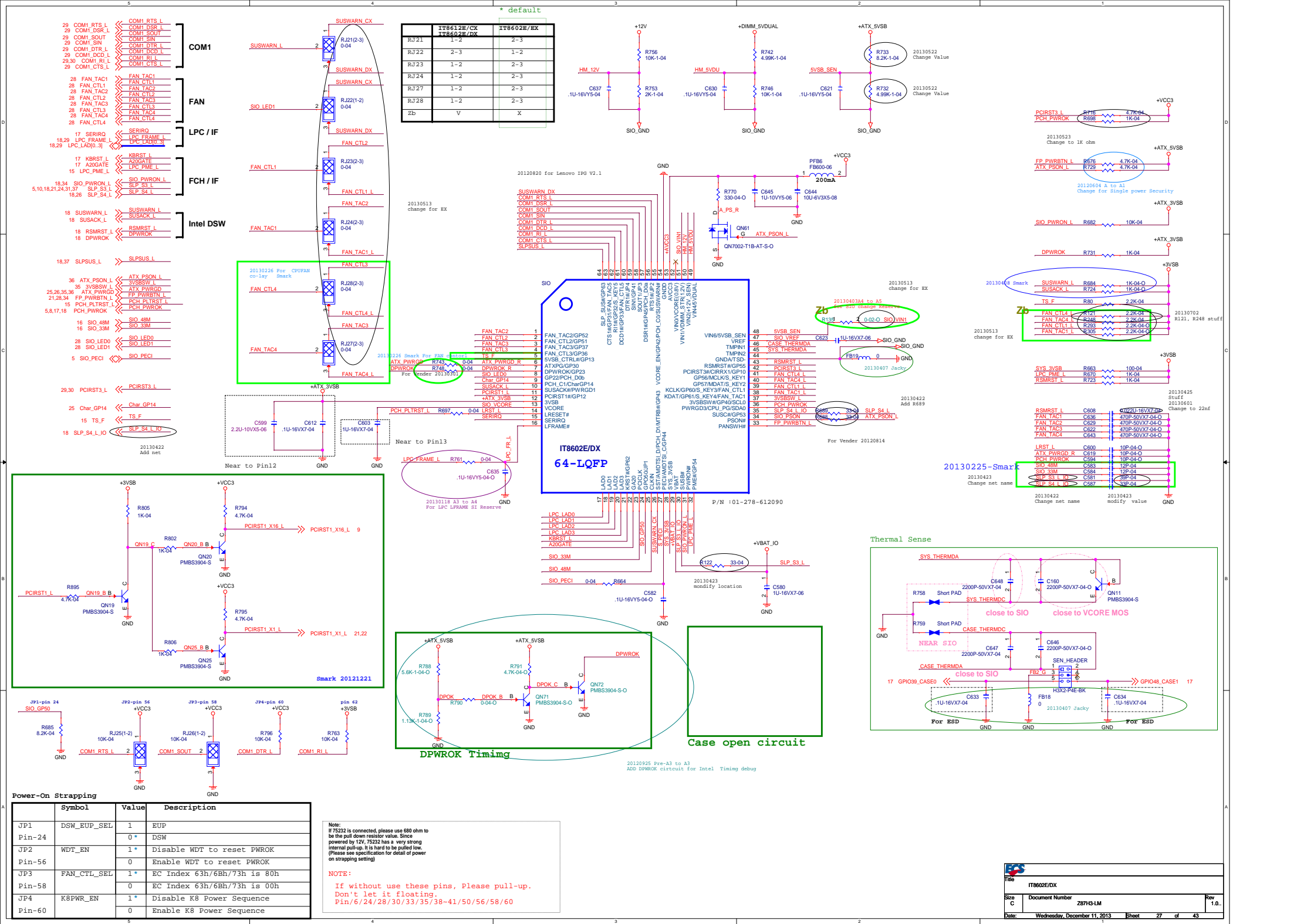


## USB3.0 Slot of USB2.0 Power Option

Status	Target	
	USB Charger	Non-USB Charger
S0,S1	+VCC(I <sub>max</sub> :0.9A)	+VCC
S3	+5VSB(I <sub>max</sub> :0.9A)	+5VSB
S4,S5	+5VSB(I <sub>max</sub> :1.6A)	O
Uc	X	V
Ud	V	X

20130606  
modify current







The diagram illustrates the LPC\_DEBUG Header Circuit. It shows the connection between a 'close SUPER I/O' chip and an 'LPC\_DEBUG' chip. The SUPER I/O chip has pins for LPC\_LAD3, LPC\_LAD2, LPC\_LAD1, LPC\_LAD0, and GND. The LPC\_DEBUG chip has pins for VCC3, GND, KEY, and various signals like LPC\_FRAME\_L, PCIRST3\_L, and LPCCLK. A capacitor C664 (1U-16VX7-04-O) is connected between the LPC\_DEBUG chip and GND. The diagram also includes a note '20121024 For BHI Reserve'.

close SUPER I/O

LPC\_DEBUG

VCC3

GND

C664  
1U-16VX7-04-O

20121024 For BHI Reserve

LPC\_LAD3

LPC\_LAD2

LPC\_LAD1

LPC\_LAD0

GND

LPC\_FRAME\_L

PCIRST3\_L

LPCCLK

KEY

JSX2\_2MM-10P

18.27 LPC\_LAD[0..3]

## Buzzer circuit

**+V\_1P5\_MINI**

20121107 Pre-A3 to A2  
to L20 for Lemovo Require

Vout : 1.5V  
Imax : 1A  
P : 0.56W

02-344-933700

U3

PGOOD GND1

EN

VIN

VDD

VOUT

NC

APL5593AKGJ

R775  
14K-104

+V\_1P5\_MINI

V1P5MINI\_ADJ

R779  
18K-104

C673  
10U-6/3X5-08

GND

GND

GND

耐压 : 6.3V

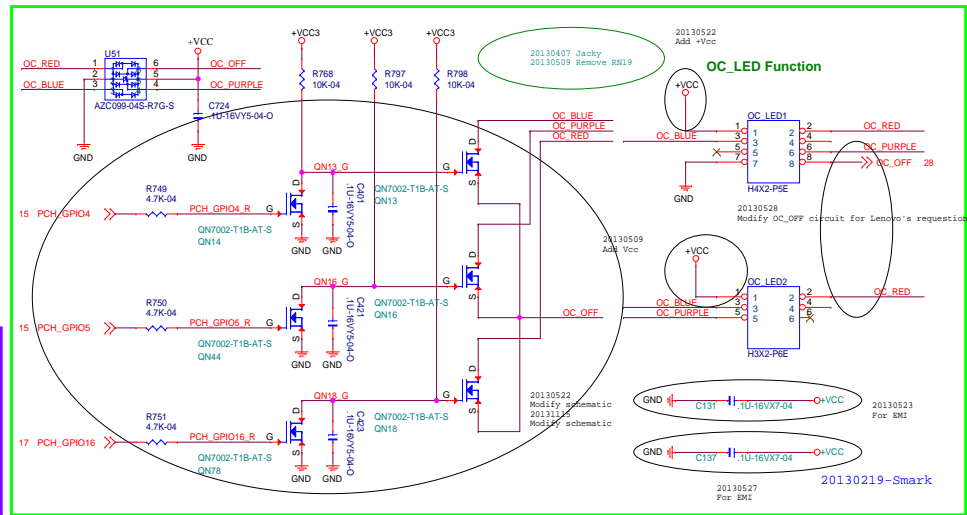
Wiring diagram for the H3X2-B-NEW-O module. The diagram shows a 6-pin connector with the following connections:

- Pin 1: GND
- Pin 2: MODE\_SWITCH
- Pin 3: MODE\_CTRL
- Pin 4: MS\_GP0
- Pin 5: MODE\_TRIGGER
- Pin 6: MS\_GP1

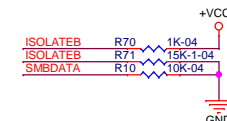
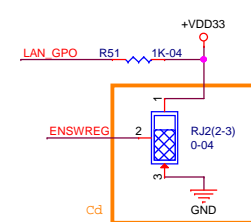
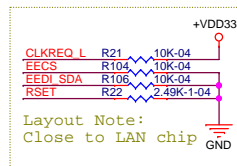
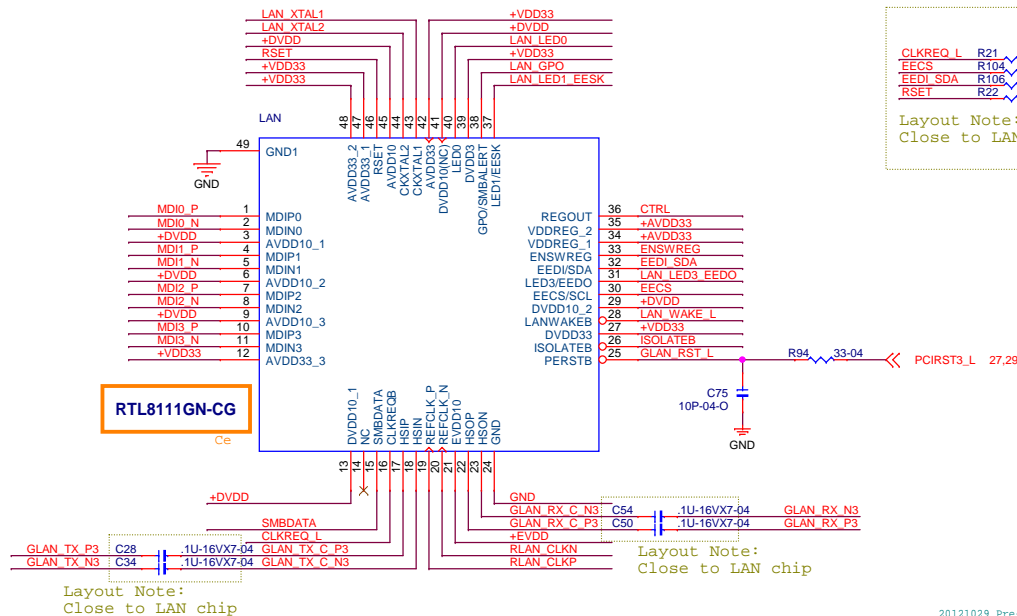
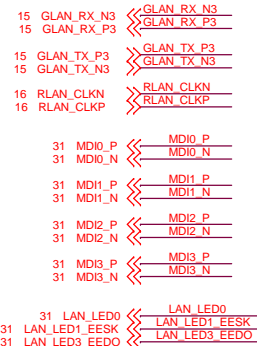
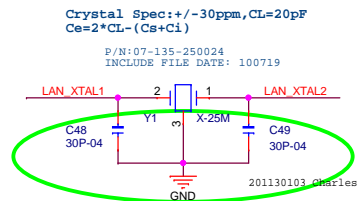
The connector is labeled "Close COM port Header".

[illegible][illegible]

	COM1_NRI_L	NRI_L
Normal	-12V	High
Active	+12V	Low

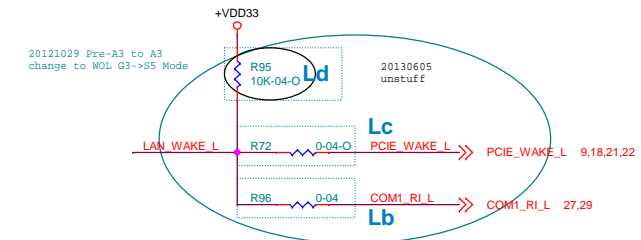






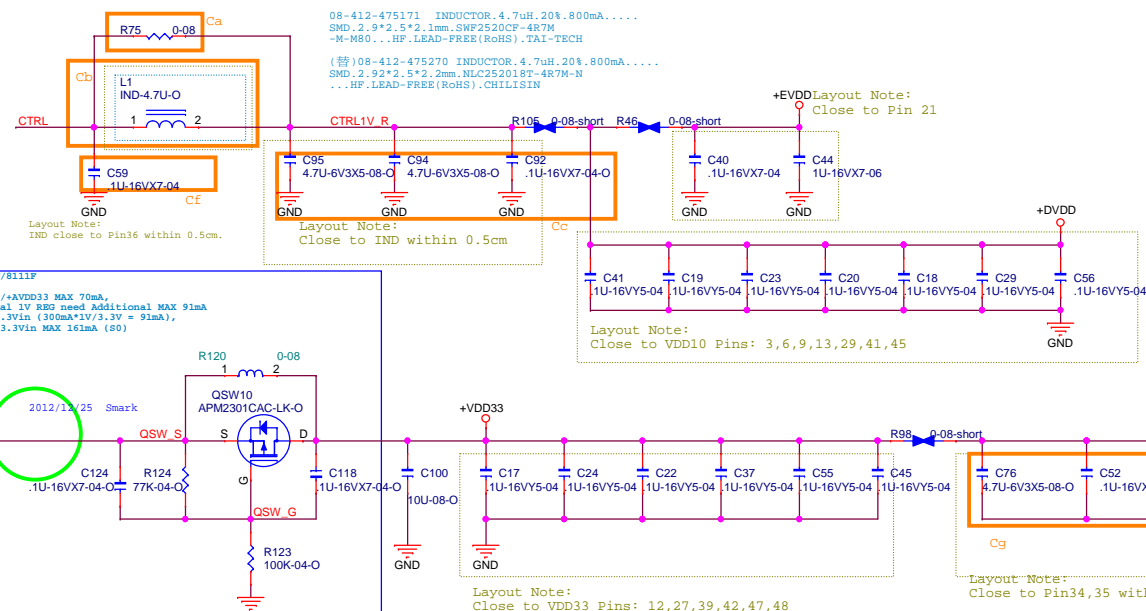
20120604 A to A1  
WOL change to Normal

MODE	Lb	Lc	Ld
WOL Normal	X	V	X
WOL G3->S5	V	X	V
WO_PCIEs G3->S5	V	V	X



## Internal Switching Regulator

8111F/8111GN:1V+-5% MAX 300mA



Chip/version	2-071-05 revision	Ca	Cb	Cc	Cd	Ce	Cf	Cg
* RTL8111GN-CG 01-267-111366	LDO	V	X	X	RJ21(2-3)	RTL8111GN-CG	V	X
RTL8111GN-CG	SWR	X	V	V	RJ21(1-2)	RTL8111GN-CG	X	V

Note: Power Sequence  
2012 0815 update

### 9.1. Power Sequence

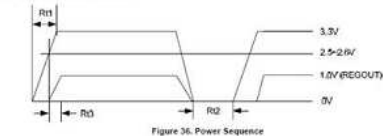


Table 2: Power Sequence Parameters

Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	0.5	-	100	ms
Rt2	3.3V Off Time	50	-	-	ms
Rt3	1.0V (REGOUT) Settle Time	-	-	15	ms

Note: See the following section for power sequence requirements.

RTL8111GN-CG

### 9. Power Sequence

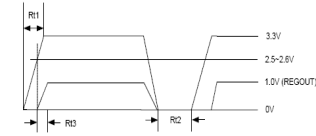
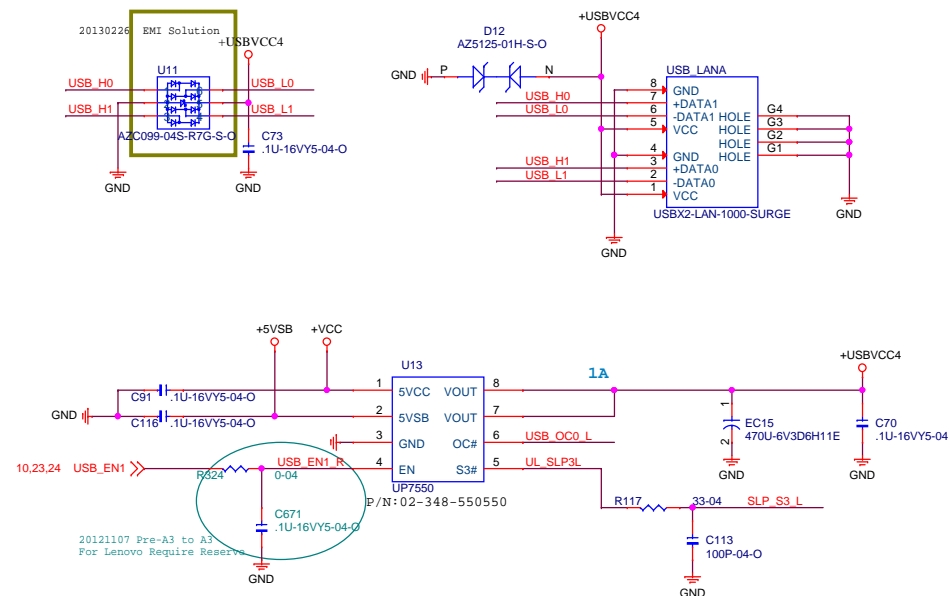


Table 19: Power Sequence Parameter

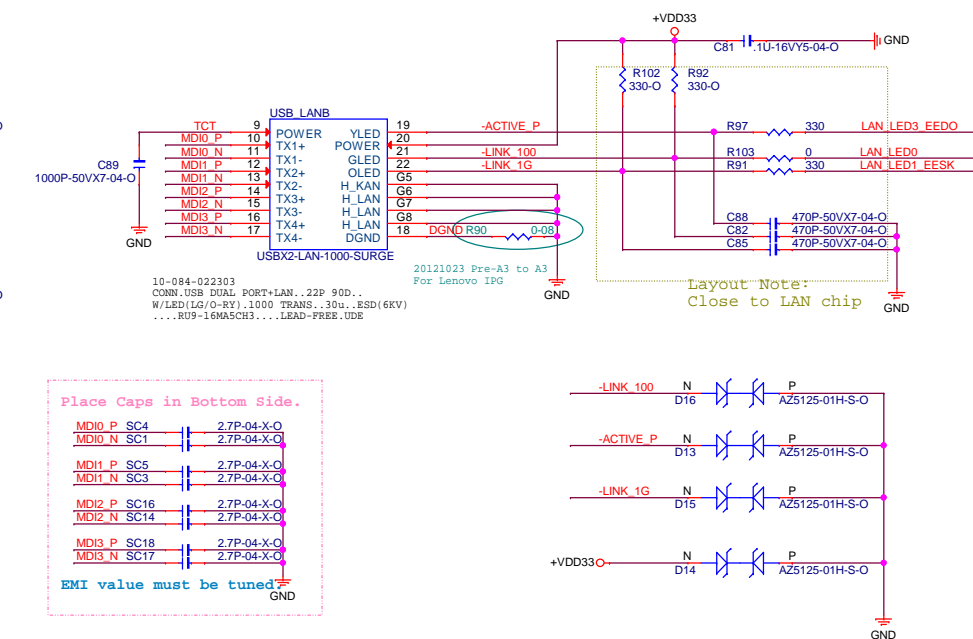
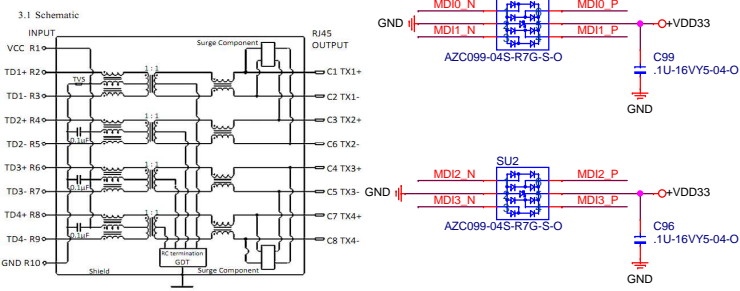
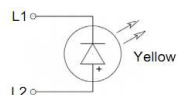
Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	0.5	-	100	ms
Rt2	3.3V Off Time	50	-	-	ms
Rt3	1.0V (REGOUT) Settle Time	-	-	15	ms

Note: See the following section for power sequence requirements.

RTL8111F-VB-CG



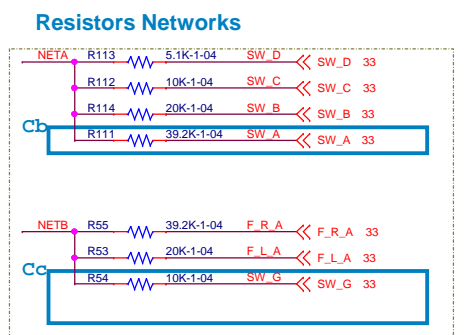
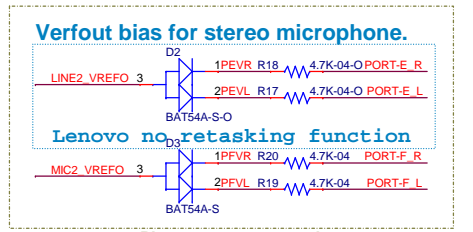
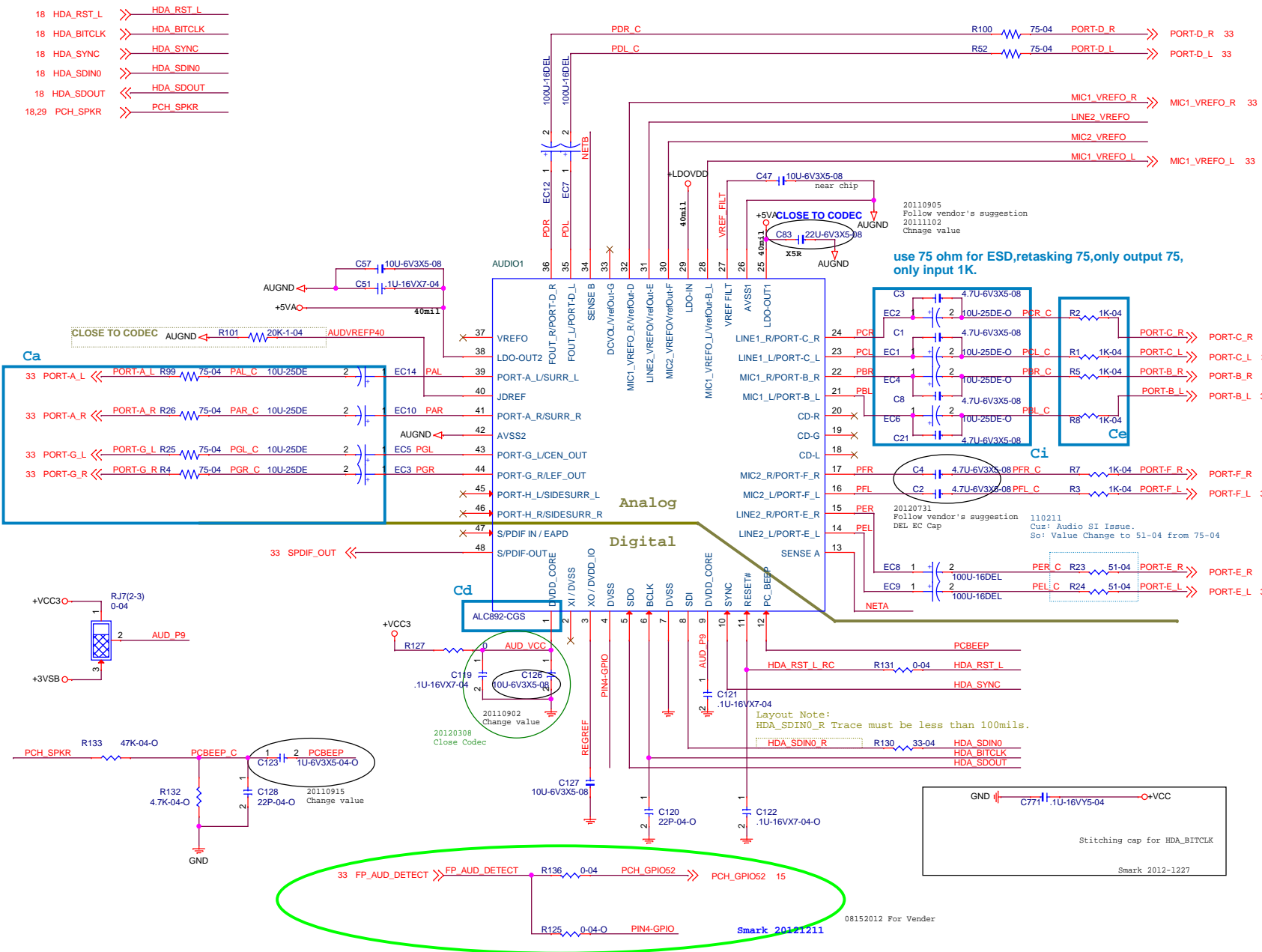
WOL	status	Yellow	Grn/Org
don't care	No Link	off	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off	off
on	10M_inactive		off
on	10M_active		off
on	100M_inactive		
on	100M_active		
on	1G_inactive		
on	1G_active		



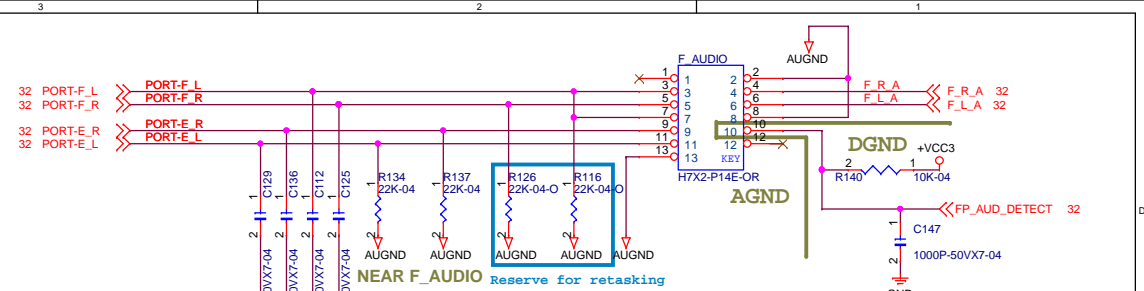
Place Caps in Bottom Side.

MDIO P	SC4	2.7P-04-X-O
MDIO N	SC1	2.7P-04-X-O
MDI1 P	SC5	2.7P-04-X-O
MDI1 N	SC3	2.7P-04-X-O
MDI2 P	SC16	2.7P-04-X-O
MDI2 N	SC14	2.7P-04-X-O
MDI3 P	SC18	2.7P-04-X-O
MDI3 N	SC17	2.7P-04-X-O

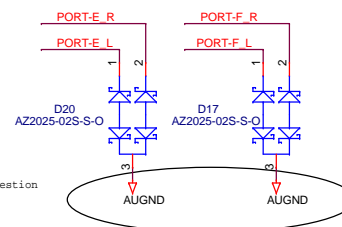
EMI value must be tuned



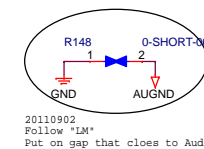
	* default	
	ALC892	ALC662-VD
Ca	V	X
Cb	v	X
Cc	V	X
Cd	ALC892-CGS	ALC662-VD-GR
Ce	1K-04	75-04
Cf	AUDIO-25P	AU-13P-BL+LI+PK
Cg	V	X
Ci	4.7U-X5-08	10U-25D4H5E
Cn	X	V



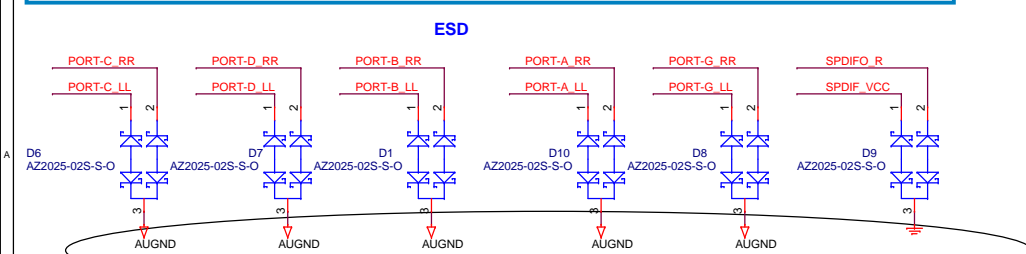
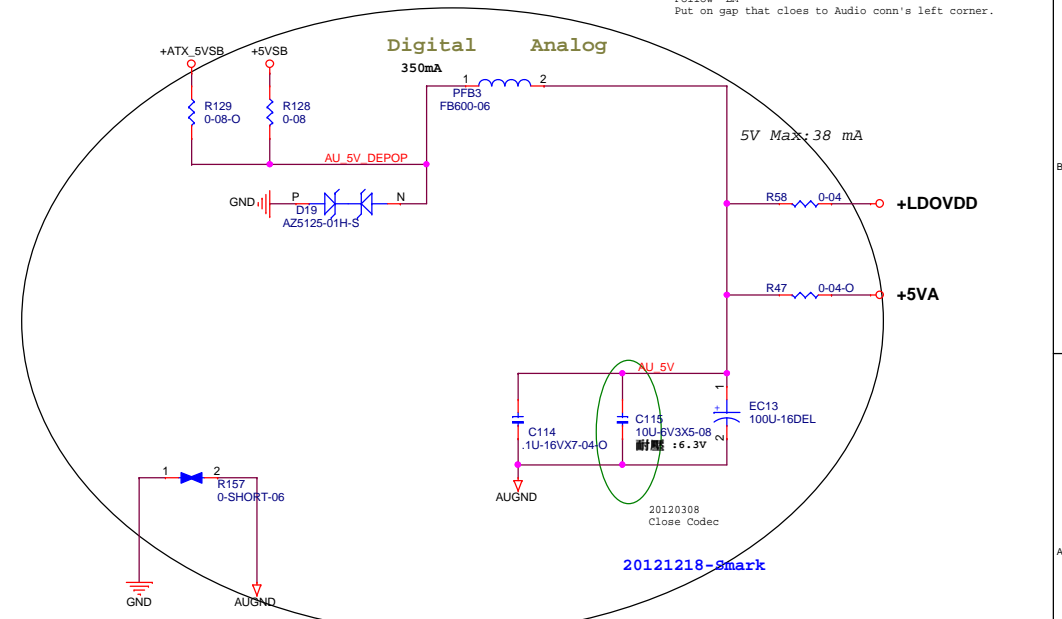
Don't put short pad too close to the rear connector.




20110905  
Follow vendor's suggestion  
20111013  
Change to analog

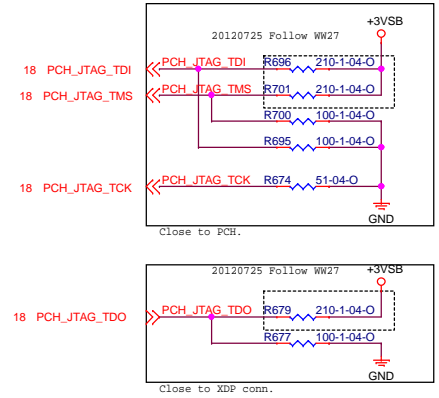
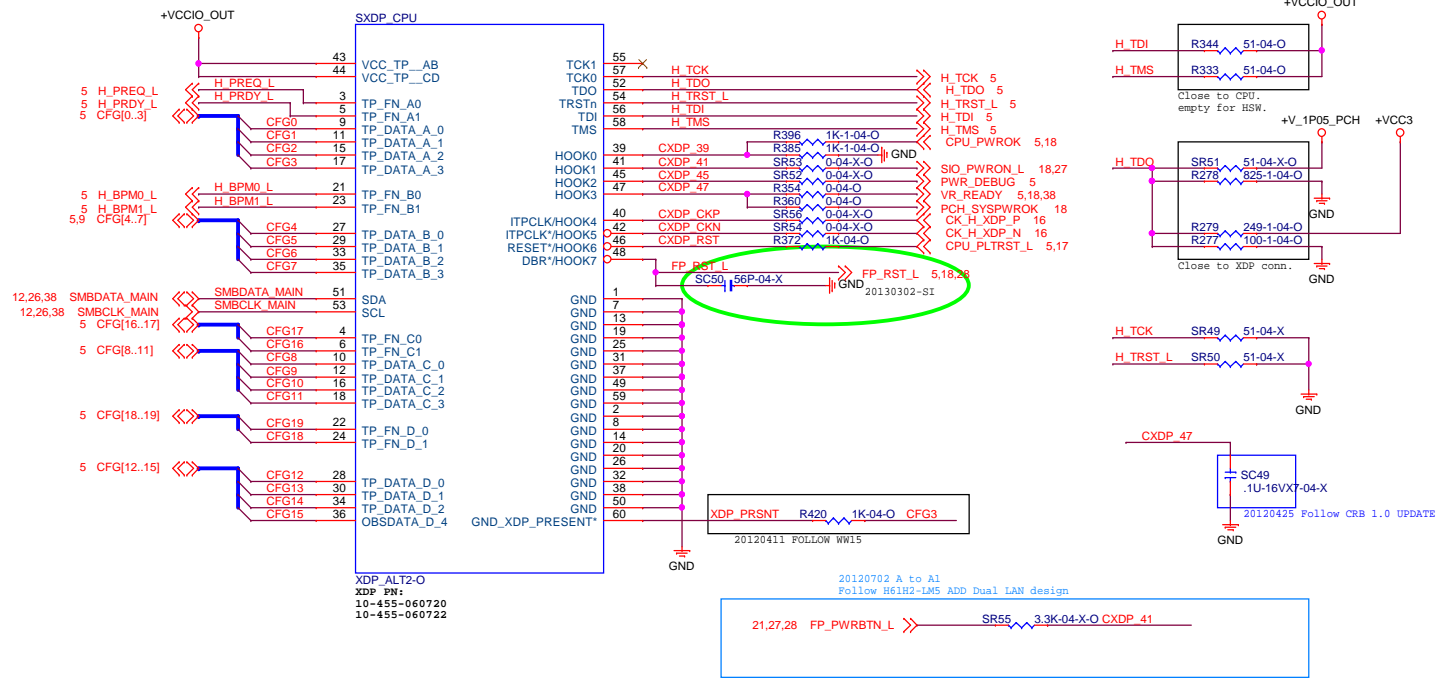


20110902  
Follow "LM"  
Put on gap that cloes to Audio conn's left corner.

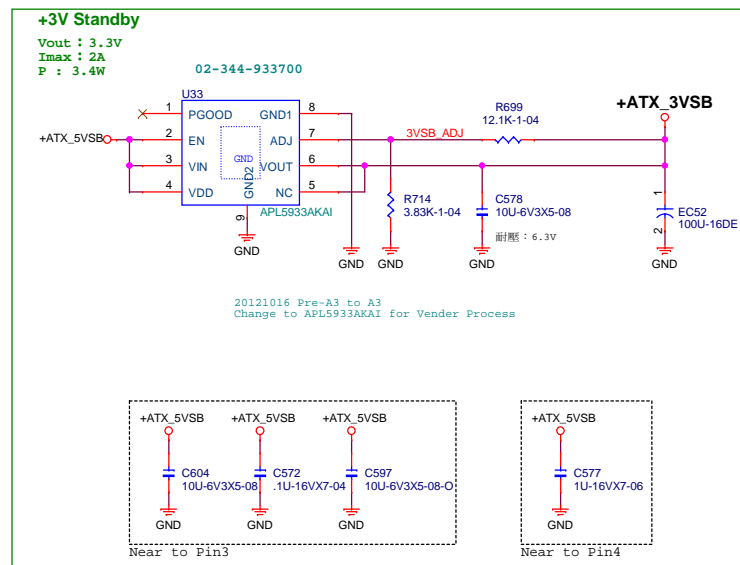
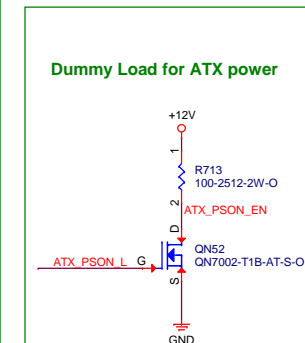
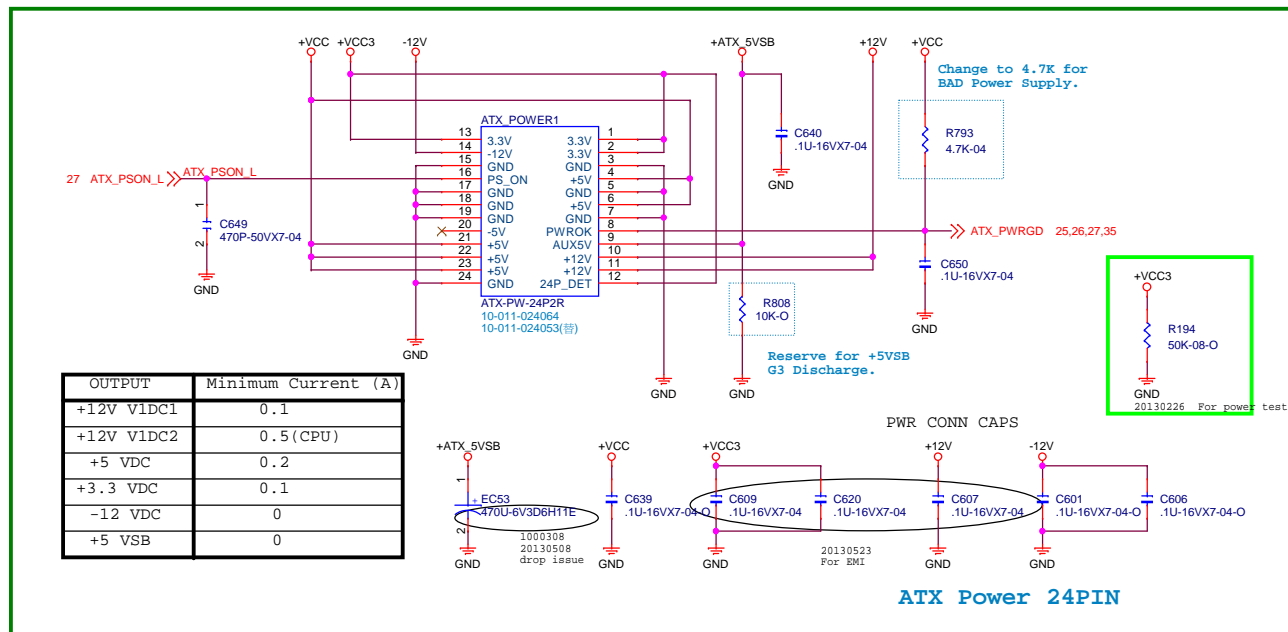


20110905  
Follow vendor's suggestion  
20111013  
Change to analog

			
Title			
AUDIO-CONN & Header			
Size	Document Number	Rev	
Custom	Z87H3-LM	1.0..	
Date:	Wednesday, December 11, 2013	Sheet	33 of 43



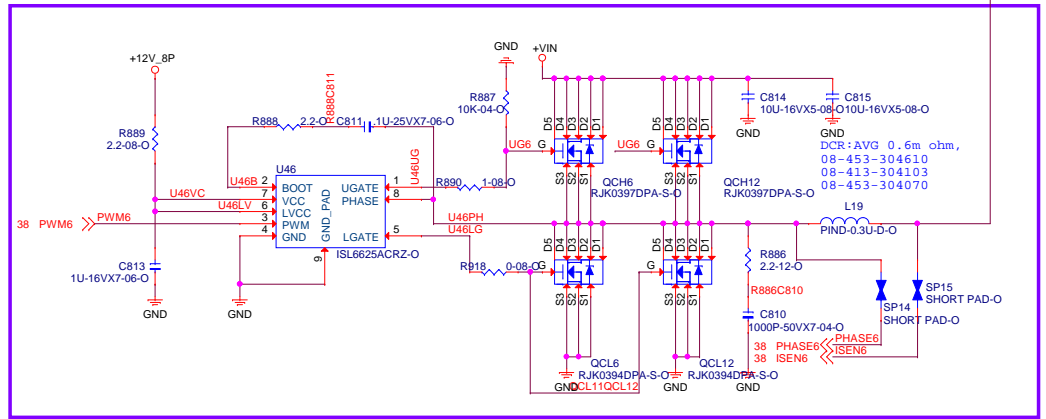
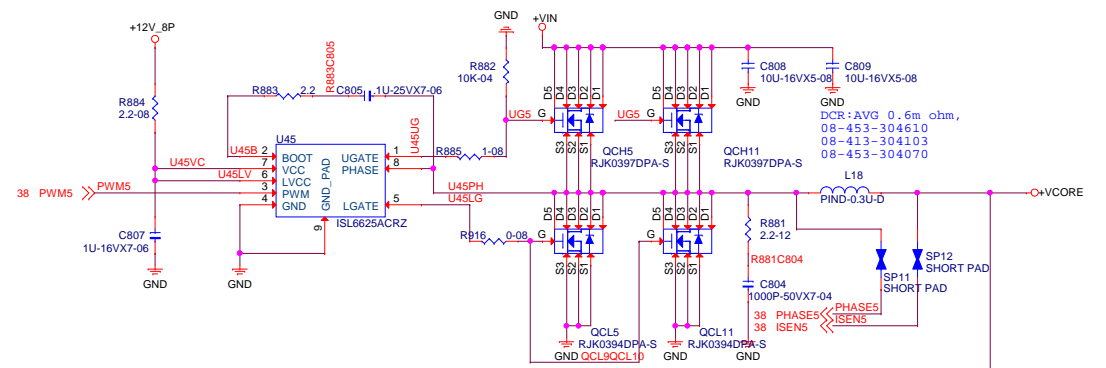
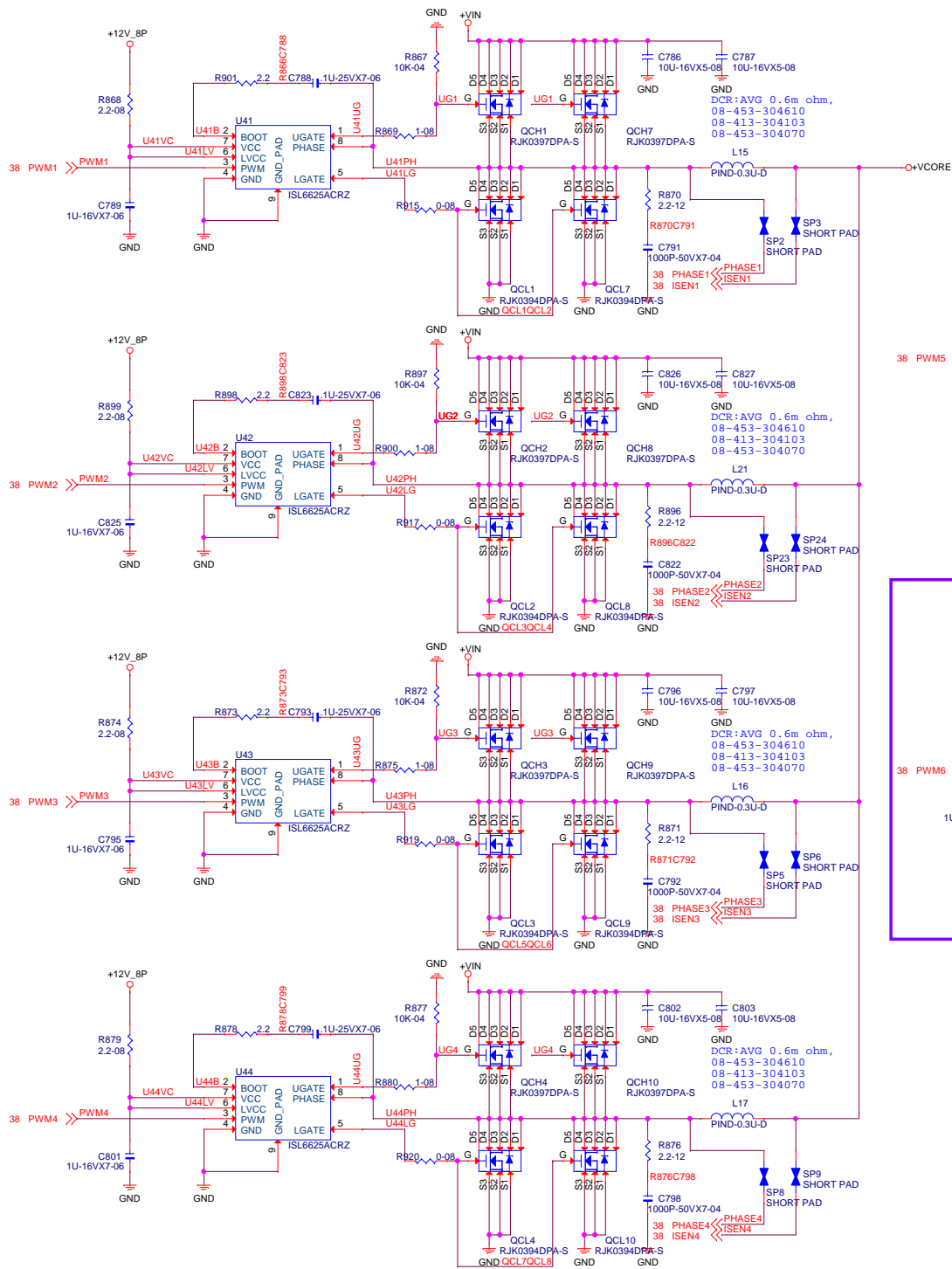




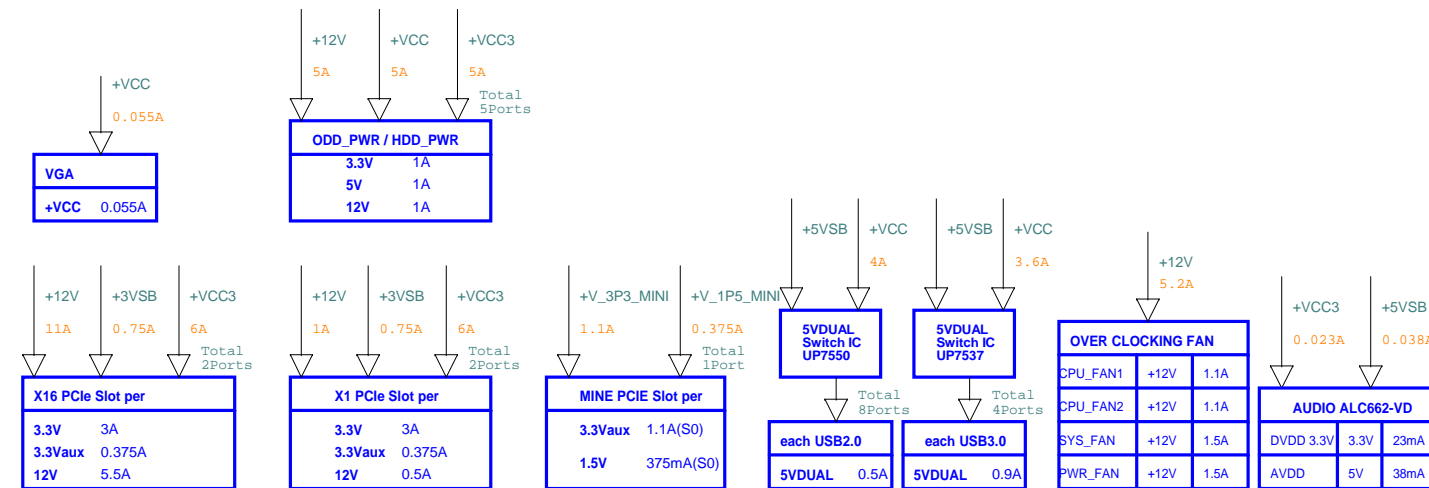
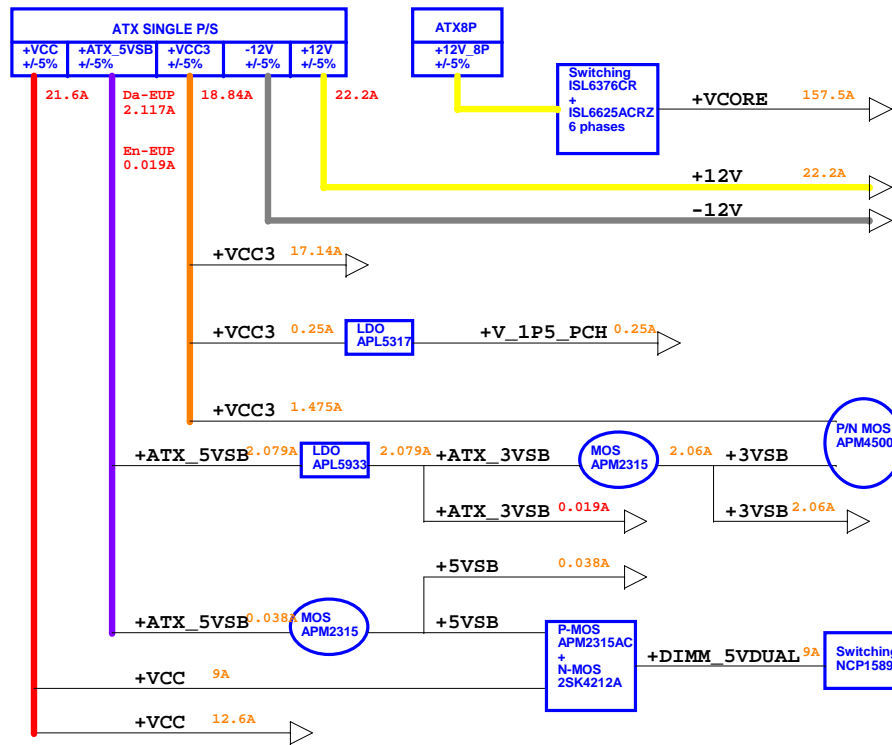








Standard Imax = 95A, Itdc = 55A  
Over clocking Imax =142.5A, Itdc = 82.5A



+VCCORE

+VDIMM

Intel Haswell CPU		
	SVID	TDC
VCORE	0.5V ~ 2.3V	70A
VDIMM	1.5V	4.5A
VCIO_PCH	1V	TBD

+VDIMM

+DDR\_VTT

DDR3 DIMM 1600MHz (4)		
V_DIMM	1.5V	16.5A
DDR_VTT	0.75V	1A

+V\_1P05\_PCH

+V\_1P05\_PCH

+V\_1P05\_PCH

+V\_1P05\_PCH

+V\_1P05\_ME

+V\_1P5\_PCH

+V\_1P5\_PCH

+VCC3

+VCC3

+VCC3

+ATX\_3VSB

+3VSB

+3VSB

+V\_1P05\_PCH

+V\_1P05\_PCH

+V\_1P05\_PCH

Intel Lynx Point (TDP 4.1W)		
VCC	1.05V	1.29A
V_PROC_IO	1.05V	4mA
VccIO	1.05V	3.629A
VccCLK	1.05V	306mA
VccASW(ME)	1.05V	670mA
VccADAC1_5	1.5V	70mA
VccVRM	1.5V	179mA
VccADAC3_3	3.3V	55mA
VccADAC3_3	3.3V	13.3mA
VccSPI	3.3V	22mA
VccDSW3_3	3VSB	15mA
VccSUS3_3	3VSB	261mA
VccSUSHDA	3VSB	10mA
DcpSUS1	1.05V	98mA
DcpSUS2	1.05V	28mA
DcpSUS3	1.05V	476mA
VccRTC	3.3V	6uA(G3)

Battery 3V

+3VSB

+ATX\_3VSB

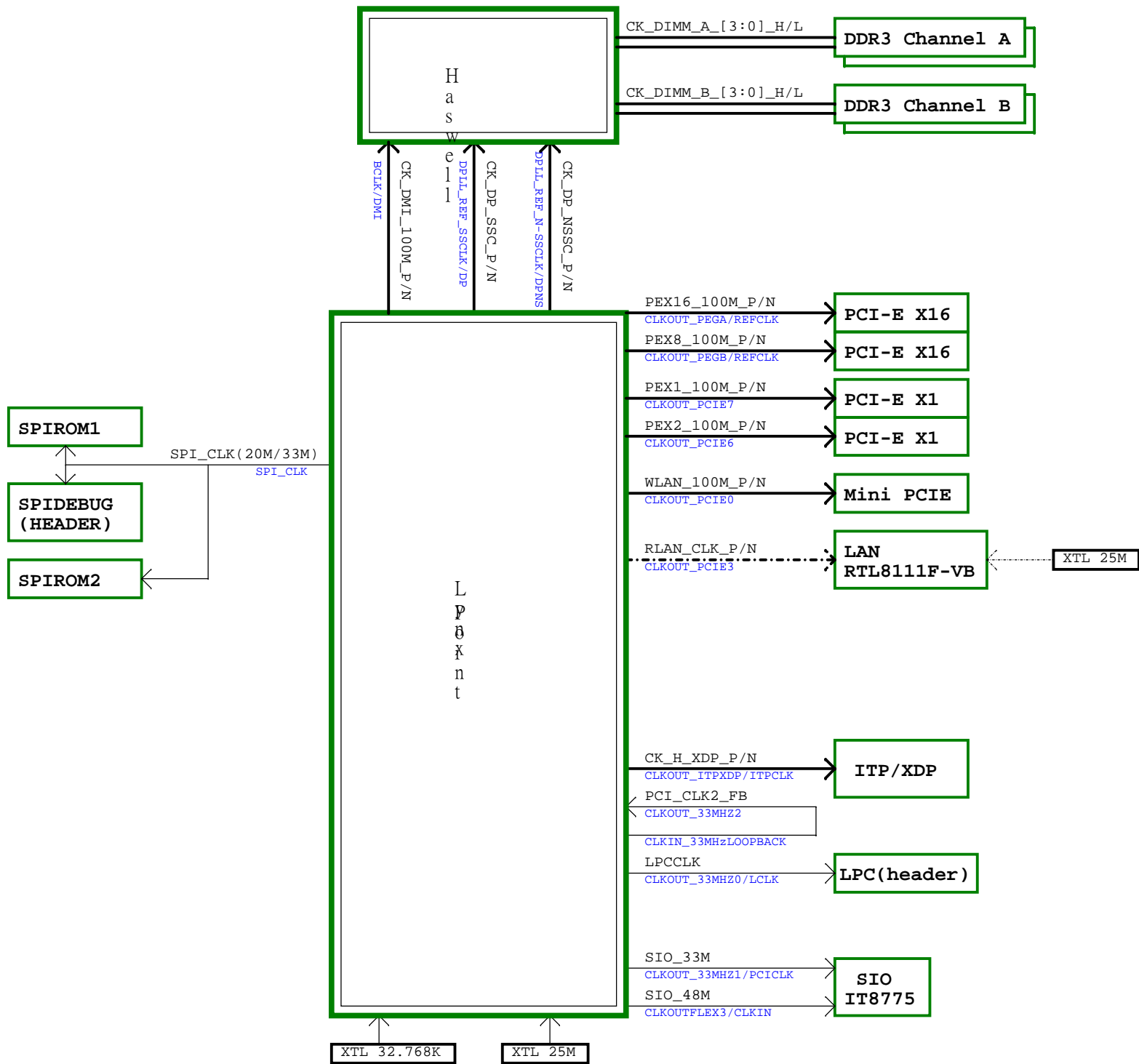
SIO IT8728/8775		
BAT 3.3V	3.3V	TBD
3VSB	3.3V	18mA
PS3VSB	3.3V	4mA

+3VSB

LAN RTL8111DGN		
VDD3P3	3.3V	272mA

PWR Delivery		
File	Document Number	Rev
Size	Custom	1.0.
Date:	Wednesday, December 11, 2013	Sheet 40 of 43





REVISION HISTORY:

Rev	Date	Notes
0.2	2012/11/26	From H81H3-LM V:A2
0.3	2013/04/10	Version 0.3 (SDV II) complete
0.4	2013/04/19	Version 0.4 (SIT) start to modify. SYSFAN_LED1 & PWEFAN_LED1 headers are changed.
0.4	2013/05/09	Modify OC_LED schematic
0.4	2013/05/13	Modify components for IT8602EX
0.5	2013/05/23	Modify OC_LED schematic
0.5	2013/05/28	Modify Block Diagram
0.5	2013/05/28	P.38: Modify R331. R345 value (follow CRB), and modify C286 location
0.5	2013/05/28	P.29: Modify OC_OFF circuit for Lenovo's requeston
0.5	2013/05/30	P.22: Add R595 for GPIO pull high
0.5	2013/05/30	P.18: RJ19 change to (2-3) for Lenovo Request MINI_PCIE CLKREQ
0.5	2013/05/30	P.27: C608 change to 22nF for RSMRST SI issue
0.5	2013/06/05	P.30: Delete R95 (COM1_RI_L pull-high at SIO side)
0.5	2013/06/10	P.25: Mofify charge IC status table
0.5	2013/06/10	P.18: R543 unstuff for over clocking
0.5	2013/06/10	P.18: R451 change from 10K ohm to 13K ohm for power leakage
0.5	2013/06/10	P.05: C277 change from 47pF to 220pF for SI issue
1.0	2013/06/11	P.18: Reserve R461 pull high 3VSB
1.0	2013/06/11	P.22: Remove DP components
1.0	2013/06/14	P.18: Remove R461 pull high 3VSB for Intel FAE's suggestion
1.0	2013/06/18	P.09: R204 change to 1k ohm to improve PCIE_RST signal rise time
1.0	2013/06/20	P.09: Add circuits for PCIE_RST monotonic issue
1.0	2013/06/20	P.11: Modify pull high/low resistors for ASM1442
1.0	2013/06/22	P.22: R495 stuff
1.0	2013/06/22	P.26: SPI_DEBUG header unstuff, ROM socket remove
1.0	2013/06/24	P.28: CPU_FAN2 unstuff
1.0	2013/07/02	P.27: Add two pull high resistors for CPU_FAN2 unstuff
1.0..	2013/12/05	P.29: Modify OC LED circuit for ESD issue